1-V Power Amplifier for 77-GHz automotive radar sensors in 28-nm FD-SOI CMOS technology

Radio Frequency Advanced Design Center

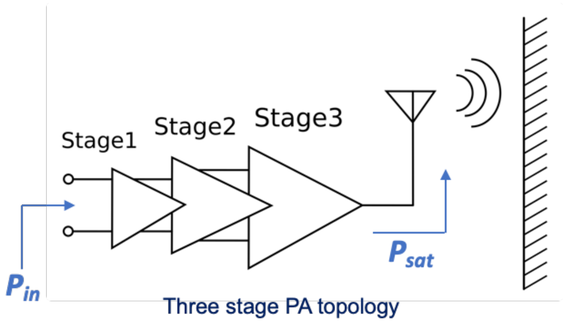
Ph.D. Student: Claudio Nocera **Tutor: Prof. Giuseppe Palmisano**

Ph.D. Brainstorming Day - Oct. 29th 2019

I.Introduction

In recent years, 77-GHz radar sensors have gained high interest due to their application in Advanced Driver Assistance Systems (ADAS). Highly scaled CMOS technologies are very promising to implement low-cost mm-wave automotive radar systems since they enable System-on-Chip (*SoC*) implementation including the mm-wave front-end, the analog base-band, and the digital processing circuitry. One of the most critical building block is the power amplifier (PA). The low breakdown voltage makes it increasingly difficult to obtain high output power levels and acceptable efficiencies. In this work, a 1-V PA for 77-GHz in 28-nm FD-SOI CMOS technology based on 3-stages common-source differential topology is described.

II. PA Topology

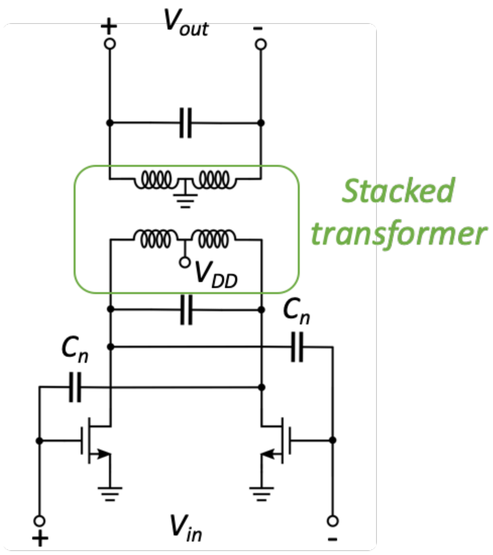


Three stage PA topology

The figure shows a simplified schematic of the proposed PA. The three stages have been designed using a pseudo-differential common-source topology with a 1-V power supply.

Output stage has been designed to reach maximum efficiency and high saturated output power, while the other stages guarantee adequate gain. Furthermore, the parasitic losses are minimized and the system has been designed with low voltage swings for low breakdown devices.

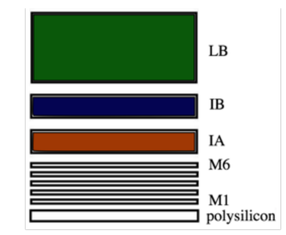
Each stage has been designed using capacitive cross-coupling neutralization, between drain and gate terminals of each transistor how shown in the figure on the right. It improve the stability across entire frequency since overcames the Miller effect on the gate-to-drain capacitance. A careful design of the input, output and interstage matching network is the key aspect to achive the desired performance.



Stage1 circuit with neutralizzation capacitors

III. Transformer Design

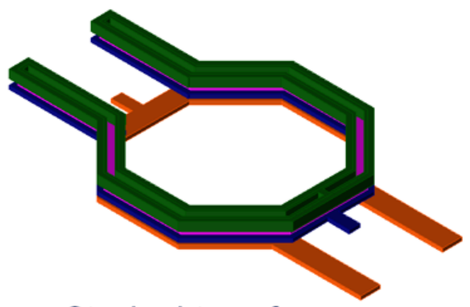
The PA has been designed in a 28-nm FD-SOI CMOS technology by STMicroelectronics. This technology uses a substrate with a not high resistivity, hence the losses have a significant impact on the performance of the PA.



Back-End-Of-Line

The back-end-of-line comprises a total of 8 copper metallization layers in addition to an aluminum cap at the top of the stack. The last three layers are used for transformer design to minimize parasitic capacitances and resistivity losses toward the substrate.

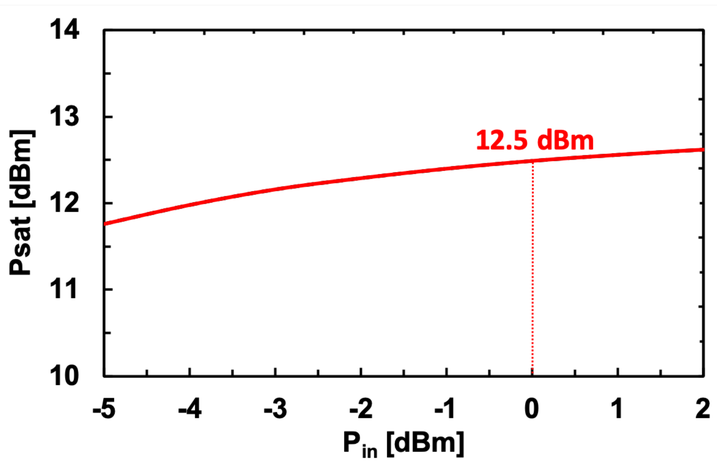
The output transformer in the first stage of the PA is based on a stacked octagonal topology. The structure has been sized to guarantee a self resonance frequency (f_{SR}) higher than twice the operating frequency. The stacked configuration exhibits a low insertion loss, (IL), thanks to a high magnetic coupling, (k).

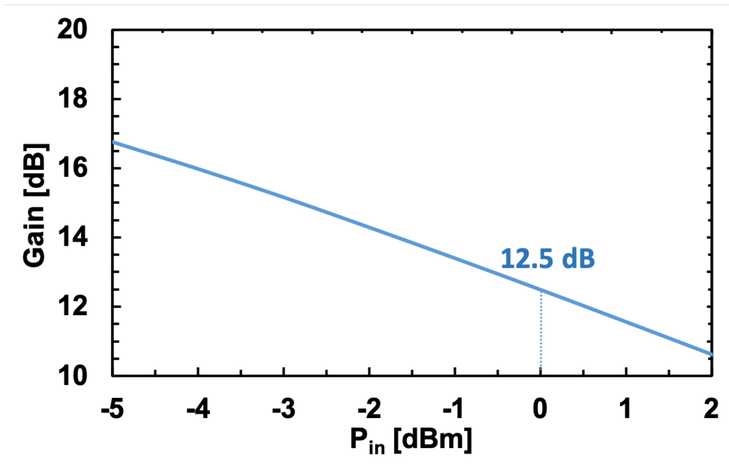

Stacked transformer

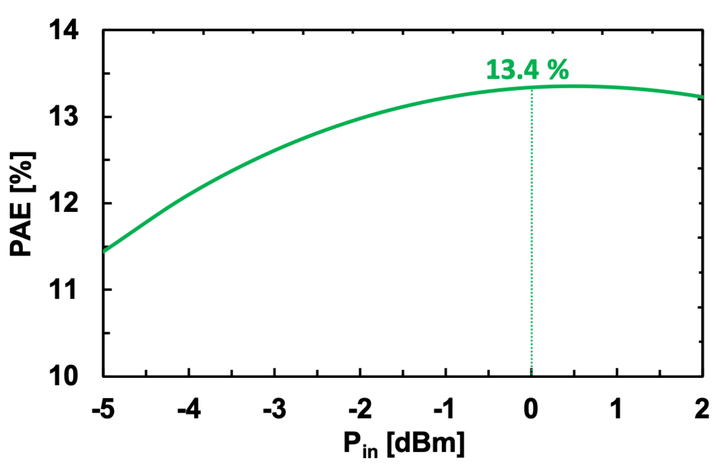
Parameters	Stacked	Units
L_P @77 GHz	84	[pH]
L_S @77 GHz	96	[pH]
Q_P @77 GHz	25	-
Q_S @77 GHz	17	-
f_{SR}	170	[GHz]
k @77 GHz	0.65	-
IL @77 GHz (in resonance)	1.3	[dB]

IV. Simulation Results

This circuit demostrates the achievement of a Long Range Radar (LRR) sensors at 77-GHz using scaled 28-nm FD-SOI CMOS technology and 1-V power supply. The importance of the gate-drain capacitances neutralization technique has been demonstrated to achive frequency stability of the PA. The power amplifier reaches a saturated output power (P_{sat}) of 12.5 dBm with a Power Added Efficienty (PAE) of 13.5% and 12.5 dB of gain with a input power (P_{in}) of 0 dBm.







V_{DD}	I_{DD}	P_{in}	P_{sat}	Gain	PAE
1 V	160 mA	0 dBm	12.5 dBm	12.5 dB	13.4%