DIEEI
Dipartimento di Ingegneria Elettrica, Elettronica e Informatica

Ultra low-power electronic systems for energy harvesting applications

Ph.D. Brainstorming day - Oct.29th 2019

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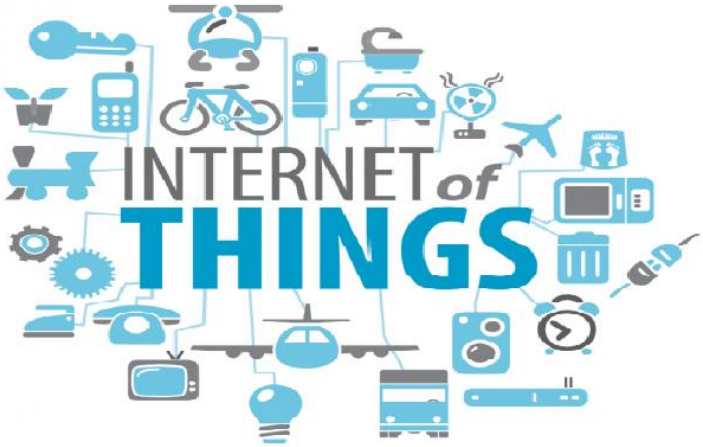
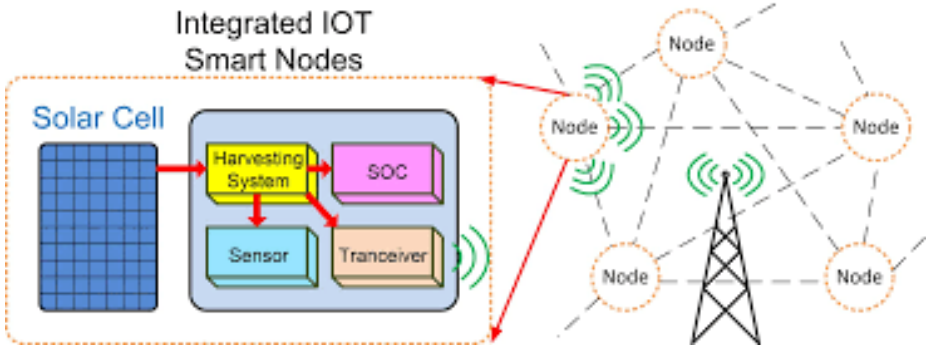
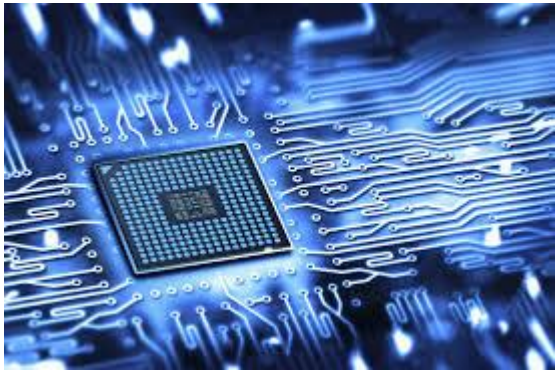
Tutor: Prof. Alfio Dario Grasso

Introduction

- **Motivations**
  - **Internet of Things (IoT)**
  - **Energy harvesting**
  - **Smart sensor nodes**
  - **Ultra low-power applications**



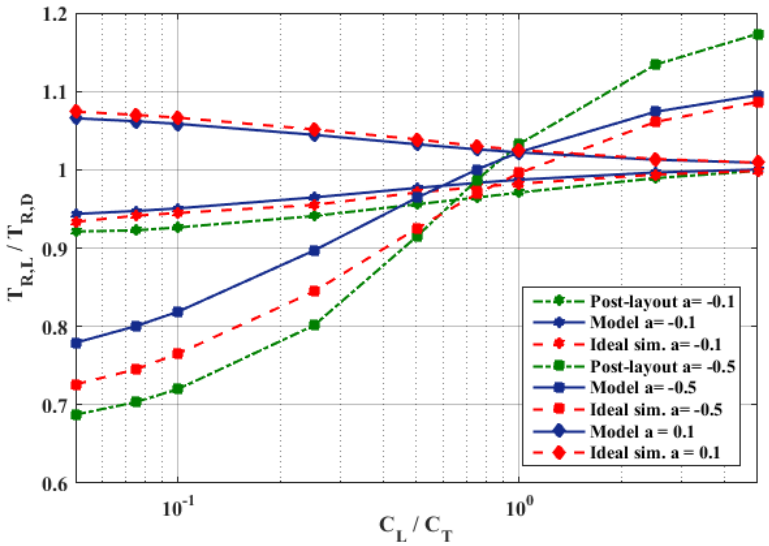


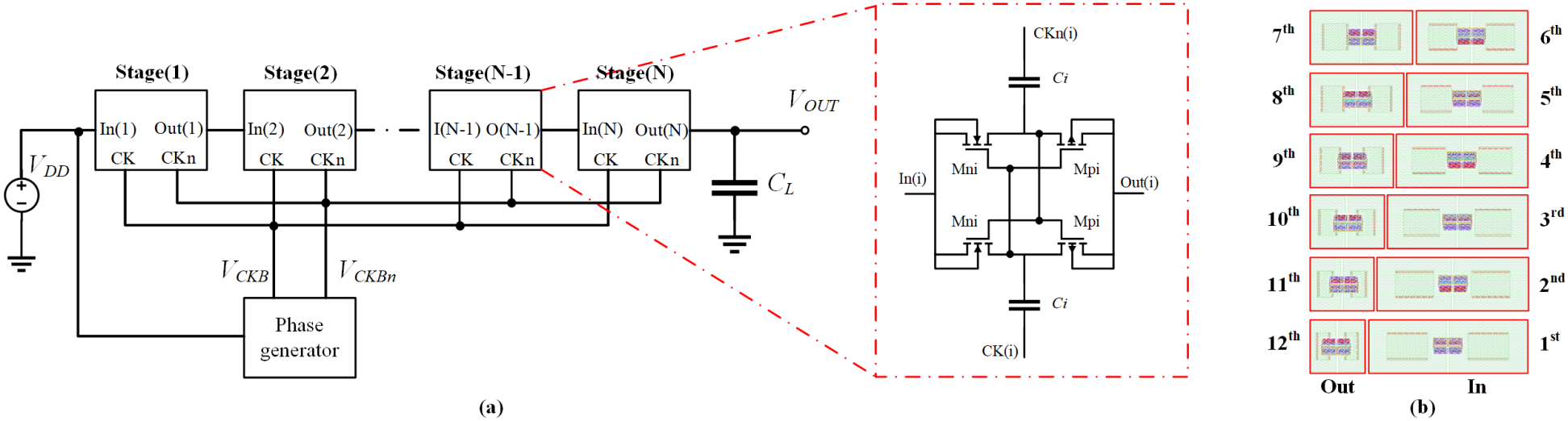


Charge Pumps: design strategy to reduce rise time

- **Proposed CP features and results**
  - High accuracy proposed model (Maximum error **lower than 12%)**
  - Rise Time reduction up to **30%**
  - Silicon Area unaltered
  - Slight increasing of the output impedance
  - Could be exploited for pure capacitive load applications

Verified on 130-nm HCMOS technology

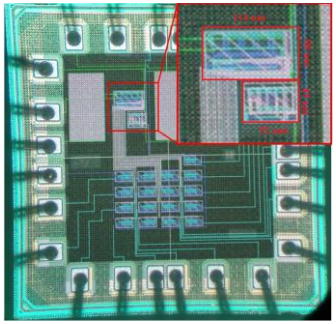




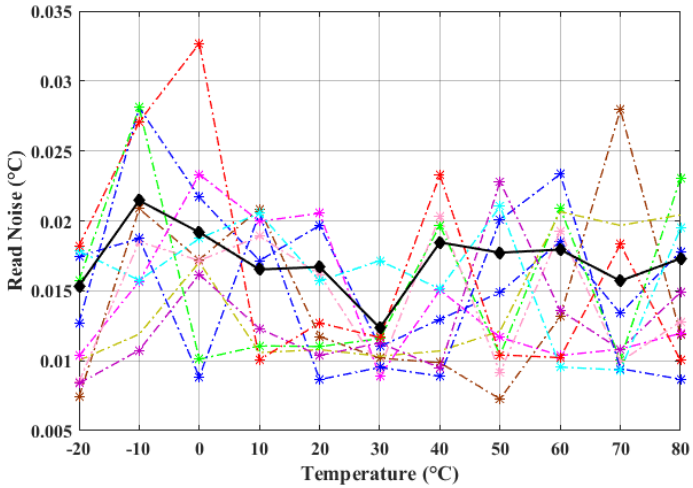
A. Ballo, A. D. Grasso, G. Palumbo and T. Tanzawa, "Linear Distribution of Capacitance in Charge Pumps to Reduce Rise Time", I.J. of Circuit Theory and applications (under review)

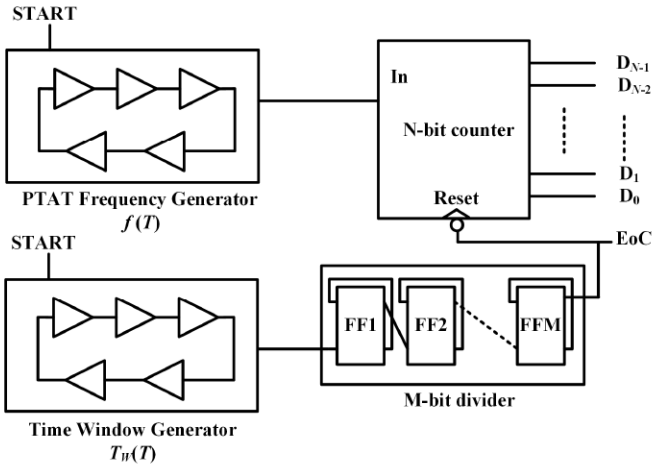
Compact ultra-low power temperature sensor

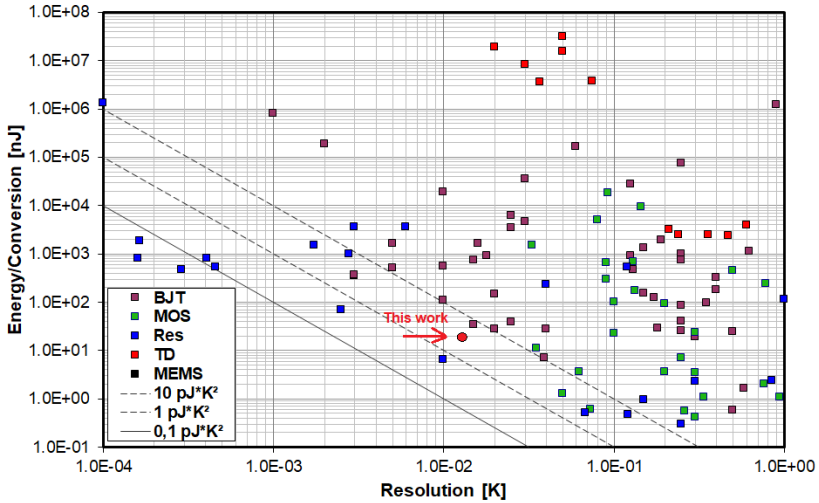
- **Sensor features**
  - Minimum power supply **V_{DD}=1,2V**
  - Measurement range **[-20, 85] °C**
  - Resolution = **12,3 mK**
  - Low power consumption **<100 nW**
  - Low Resolution-FOM = **1,82 pJ/K²**
  - Good linearity



130-nm standard CMOS technology



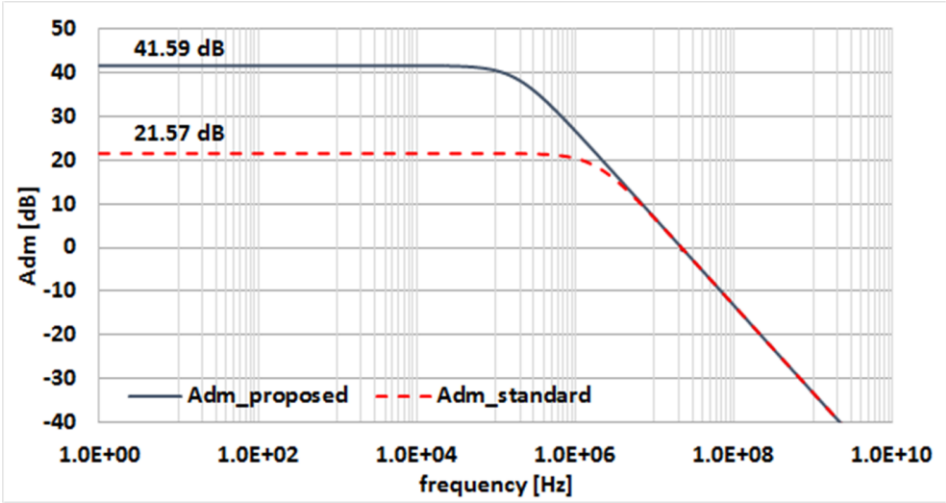


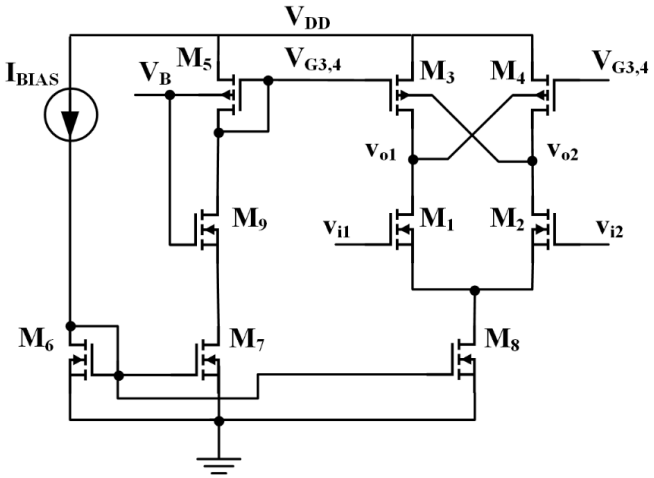


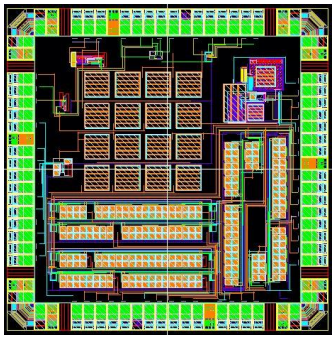
A. Ballo, G. Bruno, A. D. Grasso and M.G.G. Vaiana, "A Compact Temperature Sensor with a Resolution FoM of 1.82 pJK²", IEEE Sensors Journal (under review)

Op-Amps: Exploiting bulk to improve diff.-mode gain and CMRR

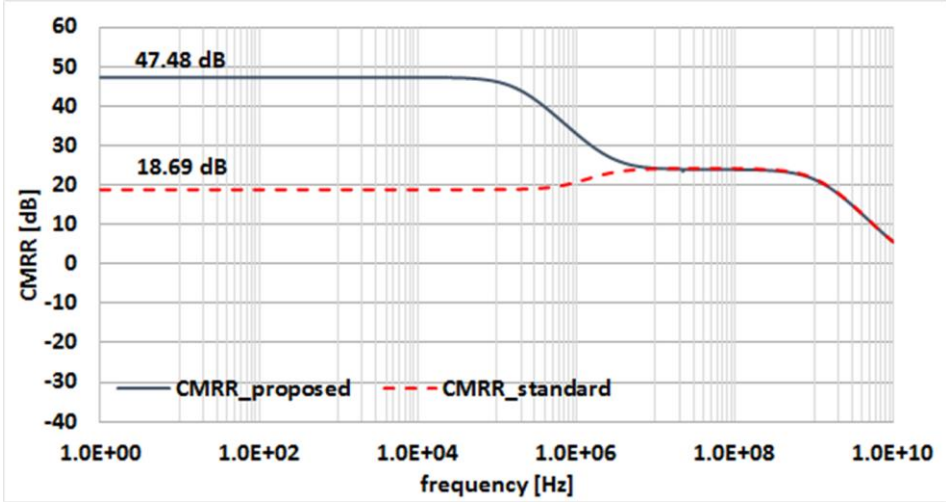
- **Proposed topology features**
  - Increasing of the output impedance
  - Improving of the **differential-mode gain**
  - Improving of the **Common Mode Rejection Ratio** (**CMRR**)
  - Silicon Area unaltered
  - Could be exploited for fully-differential solutions







Verified on 65-nm CMOS technology



A. Ballo, A. D. Grasso and S. Pennisi, "Active Load with Cross-Coupled Bulk of High-Gain High-CMRR Nanometer CMOS Differential Stages", I.J. of Circuit Theory and applications

Schools and Conferences

- International Graduate School for PhD students in Electronics, Naples, 18-20 June 2018
- 50th annual meeting of the Società Italiana Elettronica (SIE), Naples, 20-22 June 2018
- International Symposium on Integrated Circuits and Systems (ISICAS), Taormina, 2-3 September 2018
- IEEE International Conference on Electronics Circuits and Systems (ICECS), Bordeaux, 9-12 December 2018
- High Resolution Electronic Measurements in Nano-Bio Science, Milan, 8-12 April 2019

Visiting Periods

Shizuoka University, Japan, from 1st June to 2nd October 2019

Research activity: “Electronic systems for energy harvesting from photovoltaic cells in ultra-low power applications”

Publications

- *A. Ballo, G. Giustolisi, A. D. Grasso and G. Palumbo, ”A Clock Boosted Charge Pump with Reduced Rise Time”, IEEE ICECS 2018*
- *A. Ballo, A. D. Grasso, G. Giustolisi, and G. Palumbo, ‘Optimized Charge Pump with Clock Booster for Reduced Rise Time or Silicon Area’, IEEE Trans. Circuits Syst. II Express Briefs, pp. 1–1, 2019*
- *A. Ballo, A. D. Grasso, and G. Palumbo, ‘A Review of Charge Pump Topologies for the Power Management of IoT Nodes’, Electronics, vol. 8, no. 5, p. 480, May 2019*
- *A. Ballo, A. D. Grasso, and G. Palumbo, ‘A High-Performance Charge Pump Topology for Very-Low-Voltage Applications’, IEEE Trans. Circuits Syst. II Express Briefs, pp. 1–1, 2019*
- *A. Ballo, Grasso AD, Pennisi S. Active load with cross-coupled bulk for high-gain high-CMRR nanometer CMOS differential stages. Int J Circ Theor Appl. 2019;1–5*
- *Ballo Andrea, Grasso Alfio Dario, Palumbo Gaetano. A simple and effective design strategy to increase power conversion efficiency of linear charge pumps. Int J Circ Theor Appl. 2019;1-5*
- *A. Ballo, A. D. Grasso and S. Pennisi, ”CMOS Differential Stage with Improved DC Gain, CMRR and PSRR Performance”, IEEE ICECS 2019*
- *A. Ballo, G. Bruno, A. D. Grasso and M.G.G. Vaiana, ”A Compact Temperature Sensor with a Resolution FoM of 1.82 pJK2”, IEEE Sensors Journal (under review)*
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Thanks for your attention