



Ultra low-power electronic systems for energy harvesting applications



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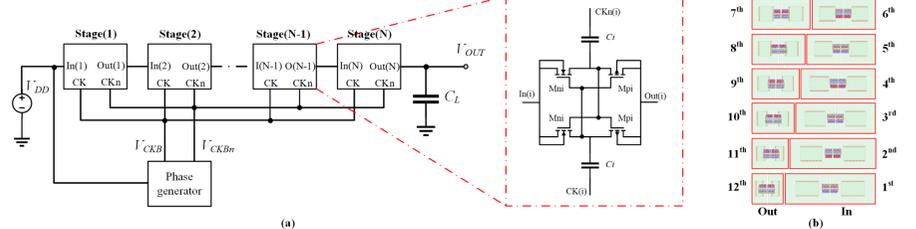
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Abstract

Nowadays **Charge pumps (CPs)**, **operational amplifiers (Op-amps)** and **thermal sensors** are ubiquitous electronic building blocks for all the integrated microelectronic circuits where power conversion, signal processing and thermal monitoring are needed features. Their use extends from μ -processor and non-volatile memory market, where they are almost always present, to the recent energy harvesting systems which constitute essential parts of implantable devices and energy-autonomous sensor nodes for the Internet-of-Things (IoT). Like for any electronic circuit, also for these blocks, power consumption, speed performance and area occupation are important design aspects and an ever-increasing number of papers dealt analysis and modelling, as well as design strategies to improve their features or proposing new performing topologies. With this in mind, we report some of the results, achieved during the last two years of research activities focused on these three blocks: as first, a Charge Pumps with a non-conventional pumping capacitance distribution is presented; as second, a low-power digital-output CMOS temperature sensor is proposed, and, as latter, a differential-pair whole active load have cross-coupled bulk is introduced.

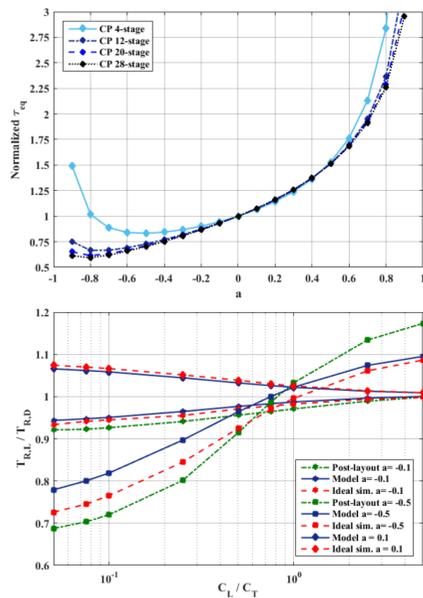
CPs: a design strategy to reduce rise time

PROPOSED DESIGN STRATEGY: the simplified block diagram of a N-stages cross-coupled dual-branch charge pump is depicted in the left side of the below figure and one of its stages is shown in the red-dashed box, in detail; otherwise, its layout is reported in the right side.



In general, the capacitors of the CP are usually designed with equal size because this choice allows to maximize the output current. However, recently it has been demonstrated that a sizing strategy which exploits different CP capacitors values can achieve benefits in term of speed performance. Although the promising results, the unique methodology proposed in literature presents the drawback of proposing an unhandy algorithm for choosing each capacitor value. In this work, we explore and propose a simple and effective linear capacitance distribution strategy which allows to design a CP with an improved rise time, getting rid of the previously mentioned issue.

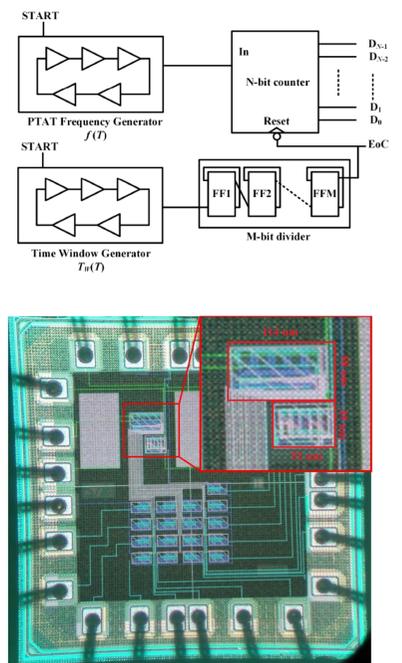
SIMULATION RESULTS AND COMPARISON: The normalized intrinsic time constant has been estimated for different number of stages and it shows that an improving could be achieved if the distribution slope "a" is negative. In order to verify its advantages, the proposed topology was simulated and its rise time was compared with that one of a traditional CP for various distribution slope and output capacitance values by using the SPICE simulator and a 130-nm CMOS technology (left plots).



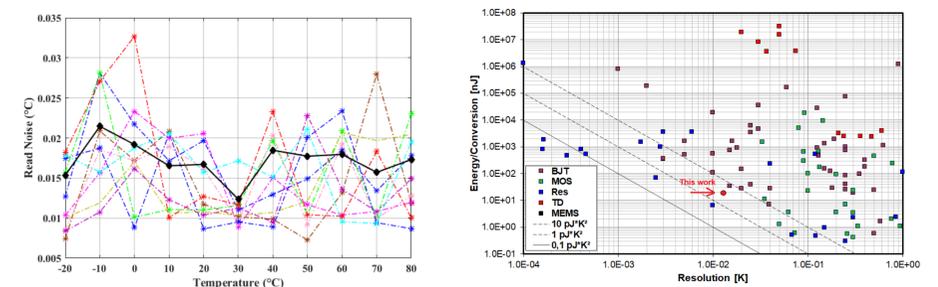
Reference: A. Ballo, A. D. Grasso, G. Palumbo and T. Tanzawa, "Linear Distribution of Capacitance in Charge Pumps to Reduce Rise Time", I.J. of Circuit Theory and applications (under review)

A compact ultra-low power temperature sensor

PROPOSED SCHEME: the simplified scheme and the micrograph of the proposed system are shown in the right side. Temperature-to-Digital conversion is based on counting a sensing oscillator, where frequency, $f(T)$, of its output is Proportional to Absolute Temperature (PTAT), during a single time window $T_W(T)$. Two different frequency PTAT square-wave signals are generated by Current Controlled Ring Oscillators, one of which goes through a frequency divider and provides the time window. Finally the comparison between the two signals takes place through a 15-bit counter, the output of which is a digital word that lead the acquired temperature information.



EXPERIMENTAL RESULTS: The proposed temperature sensor was fabricated using a 0.13- μ m CMOS process. It was designed for a measurement range $[-20, 85]^{\circ}\text{C}$ and powered from a 1.3-V supply. Total occupied silicon area is about 0,00916 mm^2 and the remaining is filled by 17 identic output buffers. Experimental results over 12 prototypes show an effective resolution equal to $12.3(\text{mK})_{\text{RMS}}$ at 30°C for a total dissipated power of $4.61\mu\text{A}$.



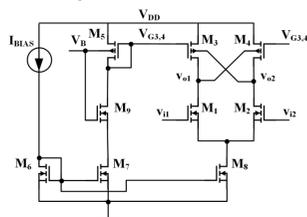
The comparison of the sensor performance with previously reported solutions is carried out using the figure of merit $\text{Resolution-FOM} = (\text{Energy/Conversion}) * \text{Resolution}^2$.

Reference: A. Ballo, G. Bruno, A. D. Grasso and M.G.G. Vaiana, "A Compact Temperature Sensor with a Resolution FoM of 1.82 pJK^2 ", IEEE Sensors Journal (under review)

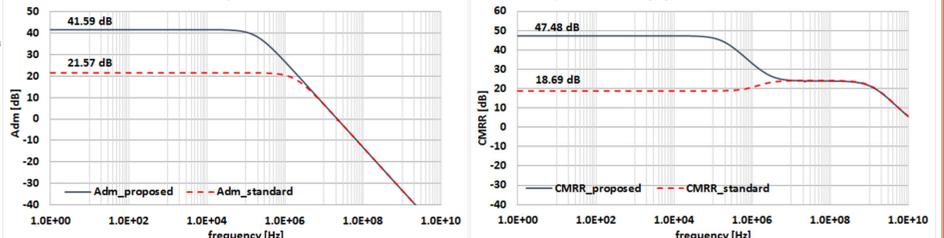
Op-Amps: Exploiting the bulk to improve differential-mode gain and CMRR

PROPOSED DESIGN: the differential pair with the proposed active load is depicted below. The bulk cross-connection causes a positive feedback loop which properties have been exploited to improve performances of the differential pair.

SIMULATION RESULTS: the solution was designed in a standard 65-nm CMOS technology and the differential-mode gain and the CMRR are reported as prove of the advantages of the proposal, as comparison with the traditional differential pair.



Reference: A. Ballo, A. D. Grasso and S. Pennisi, "Active Load with Cross-Coupled Bulk of High-Gain High-CMRR Nanometer CMOS Differential Stages", I.J. of Circuit Theory and applications



Other publications and references

- A. Ballo, A. D. Grasso and G. Palumbo, "A Review of Charge Pump Topologies for the Power Management of IoT", Electronics - MDPI Journals
- A. Ballo, A. D. Grasso, G. Palumbo, "A simple and effective design strategy to increase power conversion efficiency of linear charge pumps", International Journal of Circuit Theory and applications
- A. Ballo, A. D. Grasso and G. Palumbo, "A Review of Charge Pump Topologies for the Power Management of IoT", Electronics - MDPI Journals