Ultra low-power electronic systems for energy harvesting applications

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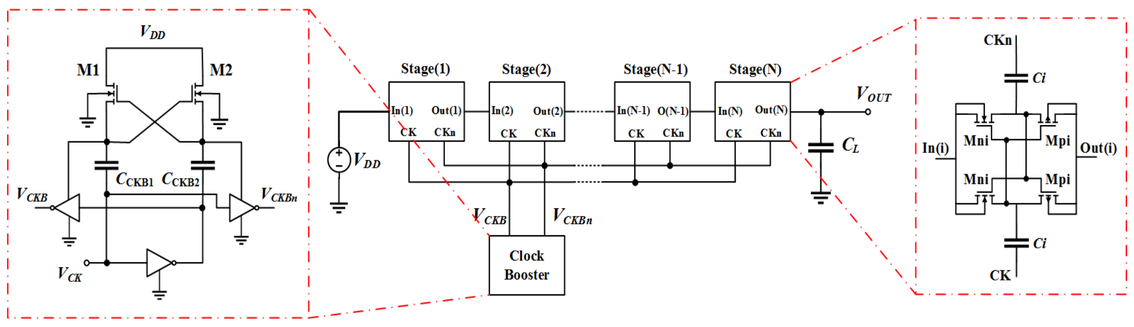
Ph.D. Brainstorming Day - Oct. 9th 2018

Abstract

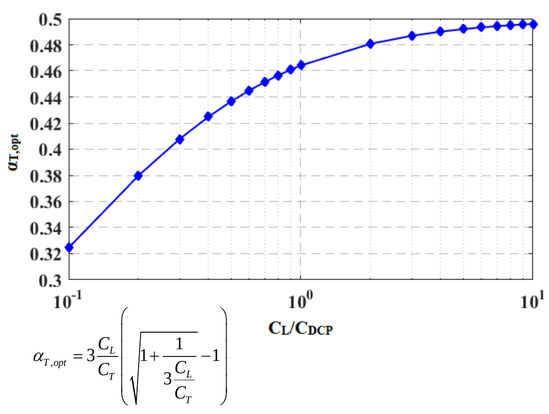
Charge pumps (CP) and **thermal sensors** are two of the most important electronic building blocks which are finding a wide application in several microelectronic circuits and embedded systems. This not only for the strongly increase in the µ-processor and non-volatile memory market, where they are almost always present, but also for their inclusion on energy harvesting systems which constitute essential parts of smart sensors and the emerging Internet-of-Things (IoT) devices. Like for any electronic circuit, speed performance, area occupation and power consumption are important design aspects, hence, some papers have dealt analysis and modelling of such blocks and also include design strategies to improve their features or propose new performing topologies. With this in mind, we present two different activities: in the first one, we propose two design methods to size Latched CPs with Clock Booster in order to maximize the advantages in term of speed or area reduction; in the second activity, instead, a low-power digital-output CMOS temperature sensor is proposed as thermic compensator for Real Time Clock systems.

Charge Pump: System description

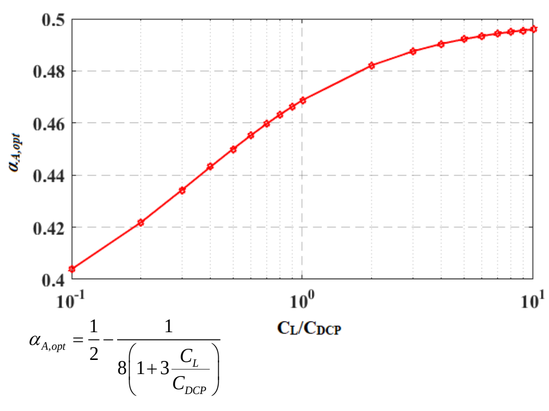
Clock boosting is a promising technique that, through clock signals amplified by a booster (CKB), allows to reduce the necessary number of stages, *N*, to guarantee output voltage constrain. Being the pump-up time proportional to N^2, it could also be significantly reduced. In real applications, however, the potential speed advantage is limited by the driving capability of CKB, hence, a sizing strategy to obviate a this drawback is investigate.



The block scheme of the whole system is plot above; in the center a N-stages latched charge pump is shown and the red-dashed box shows a voltage-doubler adopted as clock booster and a charge transfer switch, in detail. By careful analysis, supposing a pure capacitive load C_L, the pump-up time depends on the partition, *a*, of the total capacitance of the charge pump, C_{DCP}, between the sum of capacitance of the stages and clock booster's capacitors, and output capacitance. The result is the possibility to find an optimum distribution way, function of C_L/C_{DCP}, in order to minimize rise time of the output signal ($a_{T,opt}$) or, vice-versa setting the rise time, we can reduce occupation area ($a_{A,opt}$) .



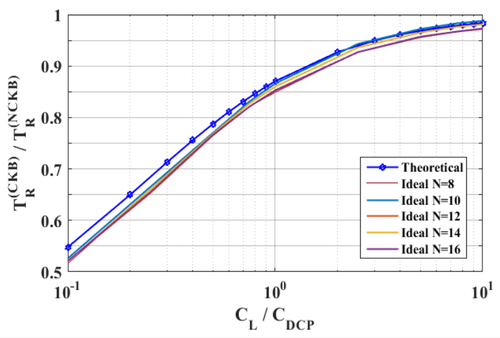
$$\alpha_{T,opt} = 3\frac{C_L}{C_T}\left(\sqrt{1+\frac{1}{3\frac{C_L}{C_T}}}-1\right)$$

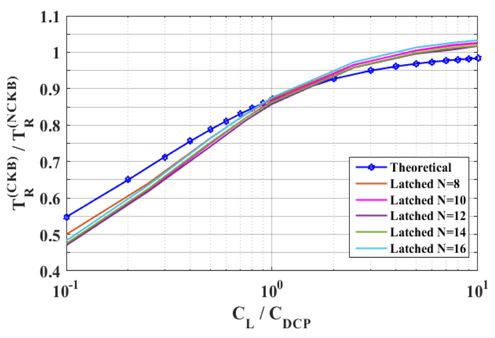


$$\alpha_{A,opt} = \frac{1}{2} - \frac{1}{8\left(1+3\frac{C_L}{C_{DCP}}\right)}$$

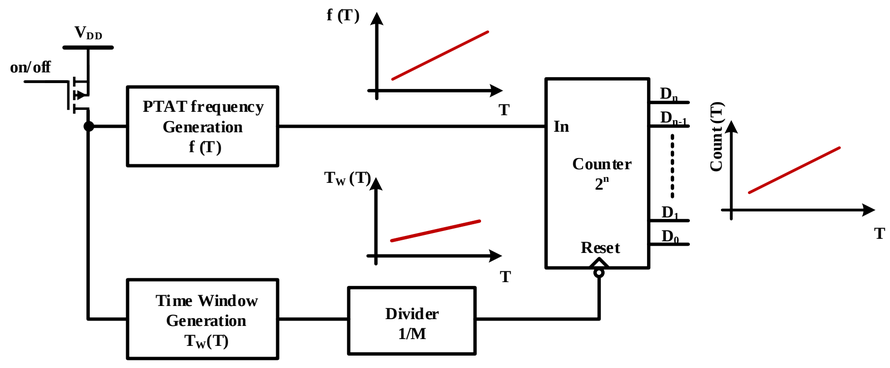
Simulation Results and comparison

To verify its advantages, the proposed topology was compared to the traditional latched CP and normalized rise time were plot. The two circuits have been simulated with different number of stages and various output capacitance values by using the SPICE simulator (left plot) and a standard 65-nm CMOS technology (right plot).





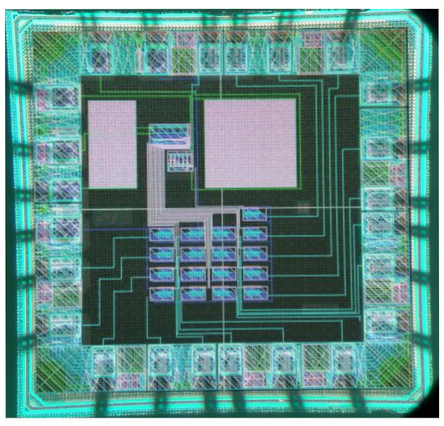
Temperature Sensor: proposed system

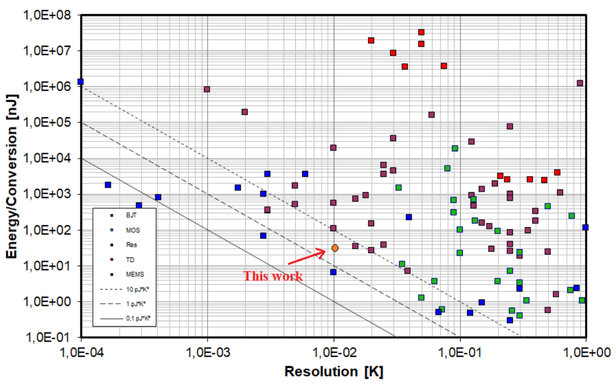


The simplified scheme of the proposed system is above depicted. Temperature-to-Digital conversion is based on counting a sensing oscillator, where frequency, f(T), of its output is Proportional to Absolute Temperature (PTAT), during a single time window $T_W(T)$. The entire circuit can be turn on/off by a p-MOSFET, used as switch, two different frequency PTAT square-wave signals are generated by Current Controlled Ring Oscillators, either goes through a frequency divider and provides the time window. Finally the comparison between the two signals take place through a 15-bit counter, the output of which is a digital word that lead the acquired temperature information.

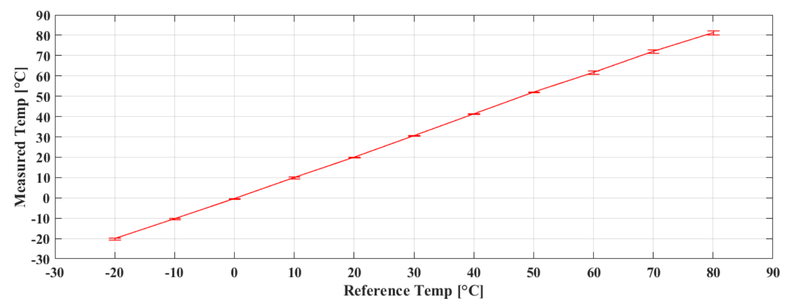
Experimental Results

The proposed temperature sensor was fabricated using a 0.13-µm CMOS process. It was designed for a measurement range [-20, 85]-°C and powered from a 1.2-V supply. Total occupied silicon area is about 0,0108 mm^2 and the remaining is filled by 17 identic output buffers. Experimental results over 12 prototypes show a shifting of the counting curves with relative standard deviation lower than 3%, while 3-σ measure error, in the worst case, is less than 1 °*C*.





The comparison of the sensor performance with previously reported solutions is carried out using the figure of merit *Resolution-FOM*=(*Energy/Conversion*)*Resolution^2.



Publications and references

A. Ballo, G. Giustolisi, A. D. Grasso and G. Palumbo, ”A Clock Boosted Charge Pump with Reduced Rise Time”, IEEE ICECS 2018

A. Ballo, G. Giustolisi, A. D. Grasso and G. Palumbo, ”Optimized Charge Pump with Clock Booster for Reduce Rise Time or Silicon Area”, IEEE Transaction on Circuit and System II: Express Briefs (under review)