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Challenges and opportunities for ultra-low power design for quantum computing applications

Dr. Sudipto Chakraborty of IBM TJ Watson Research Center
hosted by the IEEE CAS Central & South Italy Chapter

WEBINAR Link to the talk on **TEAMS** platform

Abstract: This talk will cover practical challenges for cryogenic CMOS designs for next generation quantum computing. Starting from system level, it will detail the design considerations for a non-multiplexed, semi-autonomous, transmon qubit state controller (QSC) implemented in 14nm CMOS FinFET technology. The QSC includes an augmented general-purpose digital processor that supports waveform generation and phase rotation operations combined with a low power current-mode single sideband upconversion I/Q mixer-based RF arbitrary waveform generator (AWG). Implemented in 14nm CMOS FinFET technology, the QSC generates control signals in its target 4.5GHz to 5.5 GHz frequency range, achieving an SFDR > 50dB for a signal bandwidth of 500MHz. With the controller operating in the 4K stage of a cryostat and connected to a transmon qubit in the cryostat's millikelvin stage, measured transmon T1 and T2 coherence times were 75.5µS and 73 µS, respectively, in each case comparable to results achieved using conventional room temperature controls. In further tests with transmons, a qubit-limited error rate of 7.76x10-4 per Clifford gate is achieved, again comparable to results achieved using room temperature controls. The QSC's maximum RF output power is -18 dBm, and power dissipation per qubit under active control is 23mW. An improved, low power design version that achieves half of this power will also be presented.

Sudipto Chakraborty (B. Tech, IIT, Kharagpur, 1998, Ph.D from GaTech, 2002) was with Texas Instruments till 2016 where he designed low power IC for >10 product families in automotive/wireless/medical/microcontrollers. Since 2017 he led the low power circuit design for next generation quantum computing applications in IBM research using nanometer CMOS. He has authored or co-authored >85 papers, two books and 93 US patents. He has served in the TPC including ISSCC, CICC, RFIC, IMS, and is an IBM master inventor in 2022. He serves as an AE of the (TCAS – I) and distinguished lecturer in the IEEE CASS and SSCS.