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Thesis Proposals – HR

December 2022

Nicoletta Di Noto (nicoletta.dinoto@st.com)

How to join ST

ST is Recognized as a Top Employer

ST is a top place to work in France and Italy!

We have been recognized as one of the Top Employers 2022 in Italy and France for our initiatives to improve working conditions and wellbeing, to develop competencies and grow talents and skills. It is the second year running for France and the first time for Italy.

Read the article

Added value

From theory to practice

Challenging yourself

First-hand experience within the labor market

Multicultural and challenging environment

Increasing your professional network

Investing in your professional future

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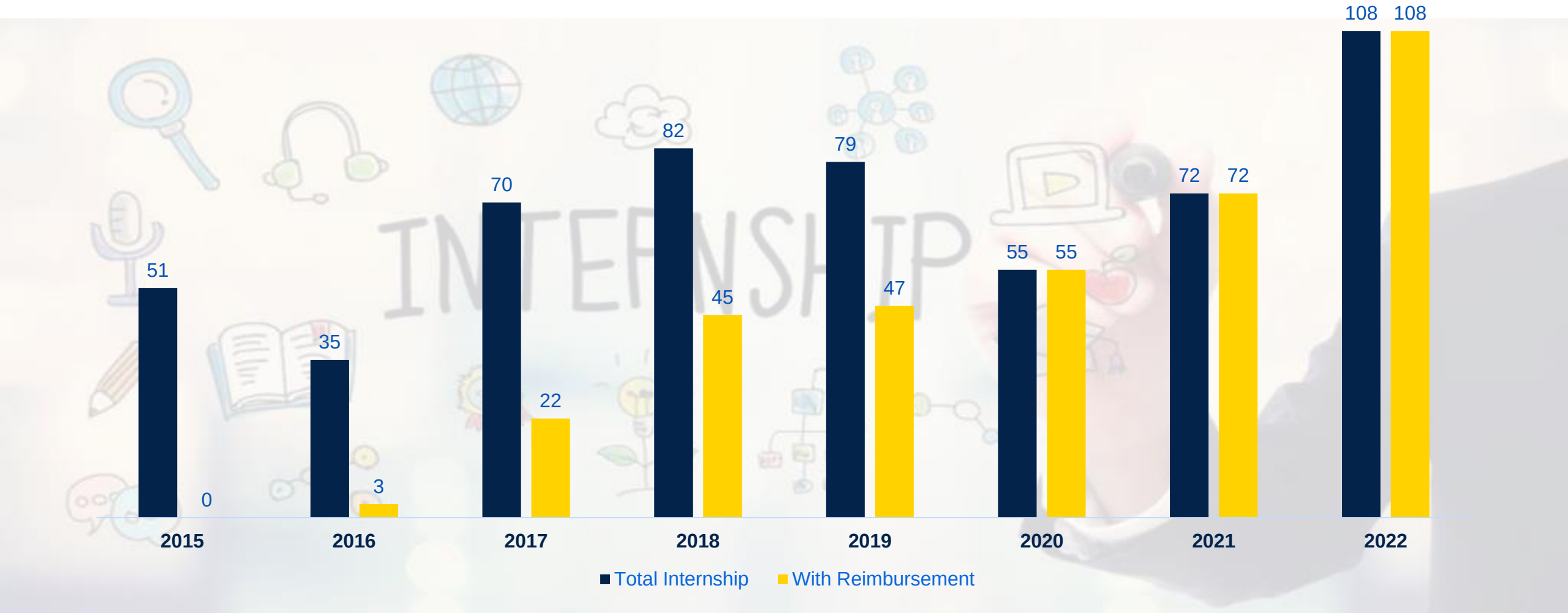
Internships



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(@ April 2022)

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Thesis Proposals - MDG

December 2022

Antonino Conte (antonino.conte@st.com)

SUGGESTED STAGES & MSc FINAL PROJECTS BY STMicroelectronics

TOPICS

- Studio ed implementazione tramite linguaggio Hardware Description Language (Verilog/VHDL) di un microcontrollore custom per memorie non volatili NVM/NVM PCM

METHODOLOGY

- Verilog
- VHDL

SEND YOUR CV BY EMAIL TO:

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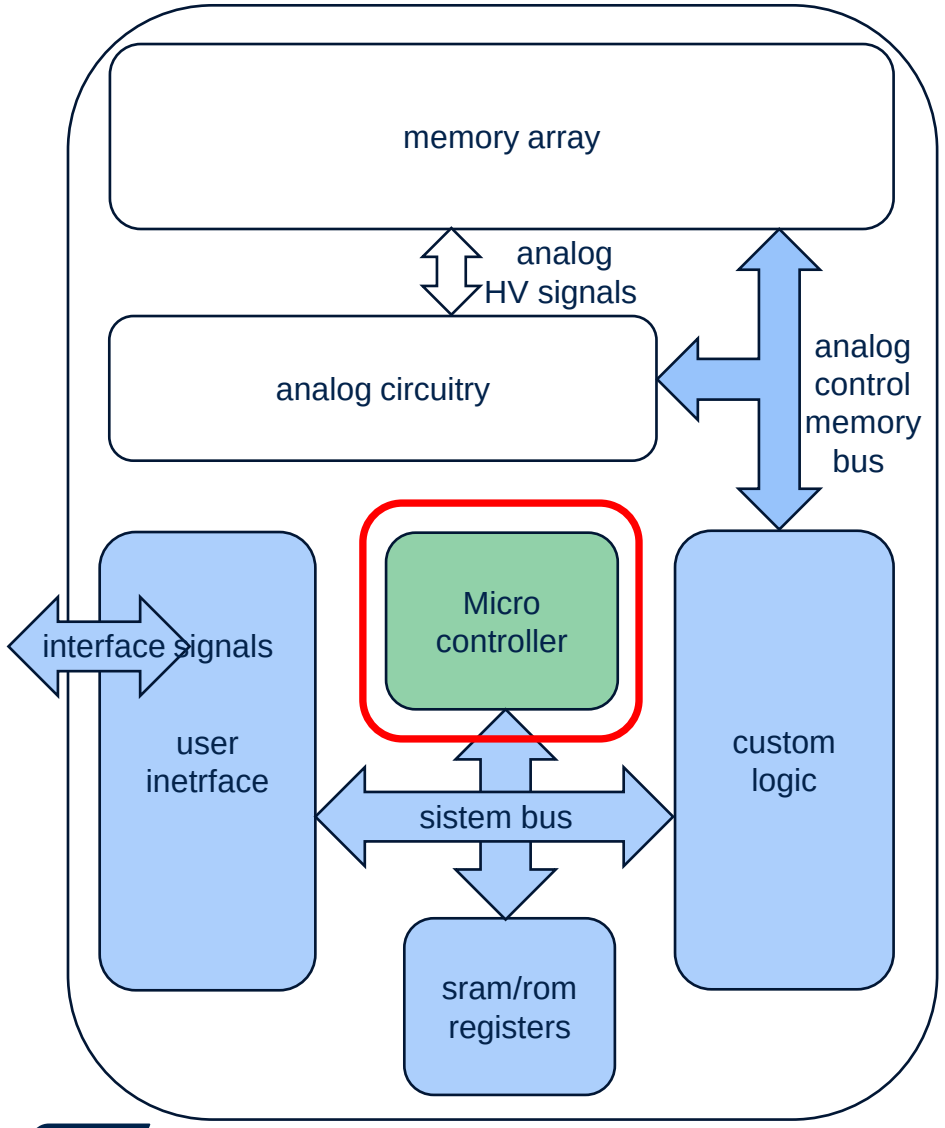
Proposta di tesi di laurea



La tesi proposta e' ***Studio ed implementazione tramite linguaggio Hardware Description Language (Verilog/VHDL) di un microcontrollore custom per memorie non volatili NVM/NVM PCM***.

Lo scopo della tesi e' lo studio di fattibilita' ed eventuale implementazione di un sequencer/micro custom ottimizzato per I circuiti di memorie non volatili.

Possibili punti chiave della tesi proposta sono:

- Studio e proposta di architettura
  - Dimensione del bus di sistema
  - Dimensione e numero di registri
  - Dimensione dello spazio di indirizzamento
  - Frequenza di sistema
- Studio e scelta del set di istruzioni
  - Opcdoes e operandi
  - Istruzioni logiche
  - Istruzioni sui segnali
  - Istruzioni di salto
- Definizione dei blocchi funzionali
- Implementazione dei blocchi funzionali

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Thesis Proposals - ADG

December 2022

Max Vizzini (max.vizzini@st.com)

SUGGESTED STAGES & MSc FINAL PROJECTS BY STMicroelectronics – ADG Central Technical Team

TOPICS

- Disabled aid / Traffic patrol aid in-vehicle acoustic warning system
- Shopping cart automatic transport
- Electronic tow hitch (towed vehicle)
- Touch-less in-vehicle control
- Electronic injection control for mixed fuel of an ICE (hydrogen, biofuel…)

METHODOLOGY

- AutoDevKit Ecosystem
- Matlab, Fusion, Inventor, Altium…
- SPC5Studio AI
- MCU full stack development

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Thesis common traits

Who we are: **Automotive and Discrete Group – Central application team**

What we do: **System solutions for transportations and ‘new mobility’ markets**

Domain of competences: **Electric, Electronic, Mechanics, Computer Science, Control, Digital Marketing, Communication**

Duration: **6 months**

Location: **On ST premises with assigned tutor**

Number of people: ***2-3***

Effort: High, it requires strong motivation

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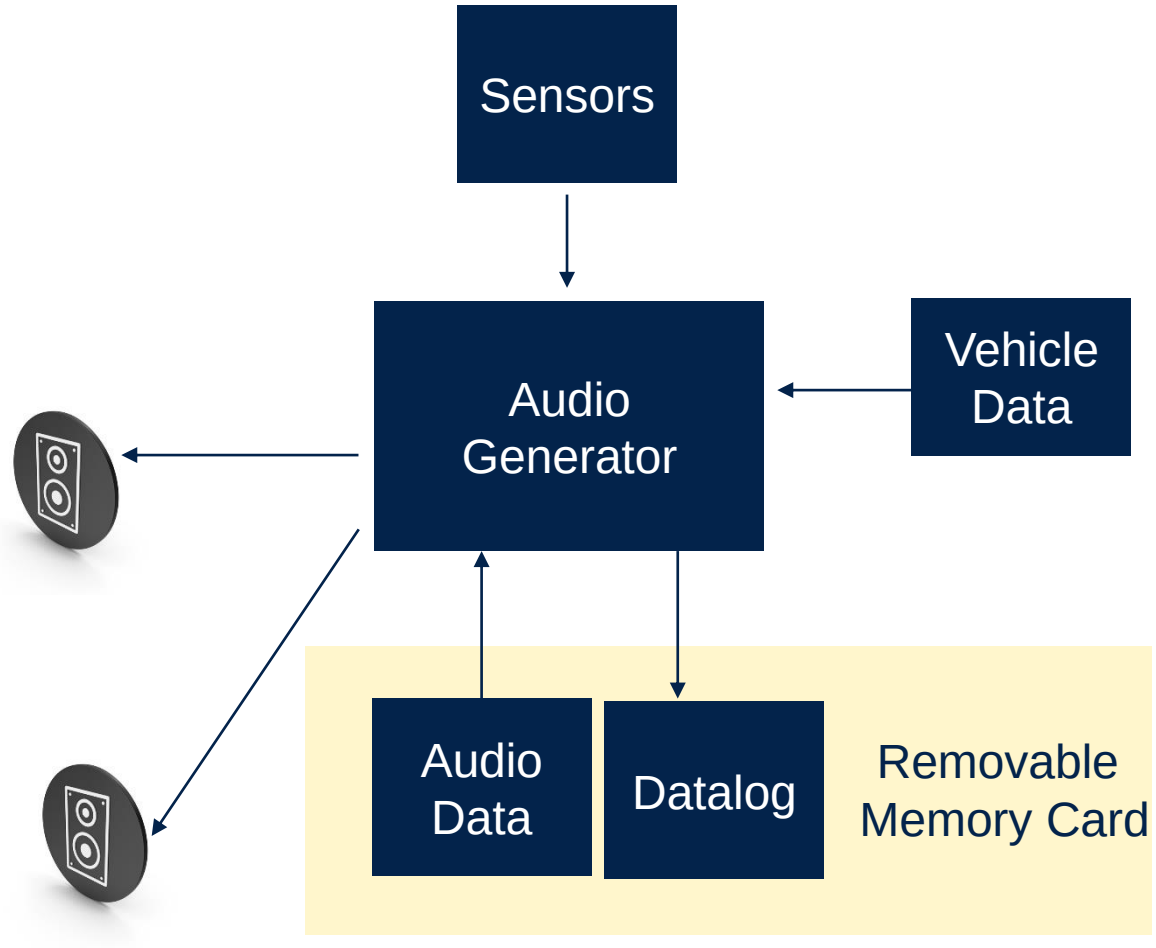
Disabled aid / Traffic patrol aid in-vehicle acoustic warning system

Key features:

- ECU-like design
- Set of pre-recorded audios & messages
- Data collection from direct sensors and via vehicle communication bus
- Data logging for incidents and near-misses



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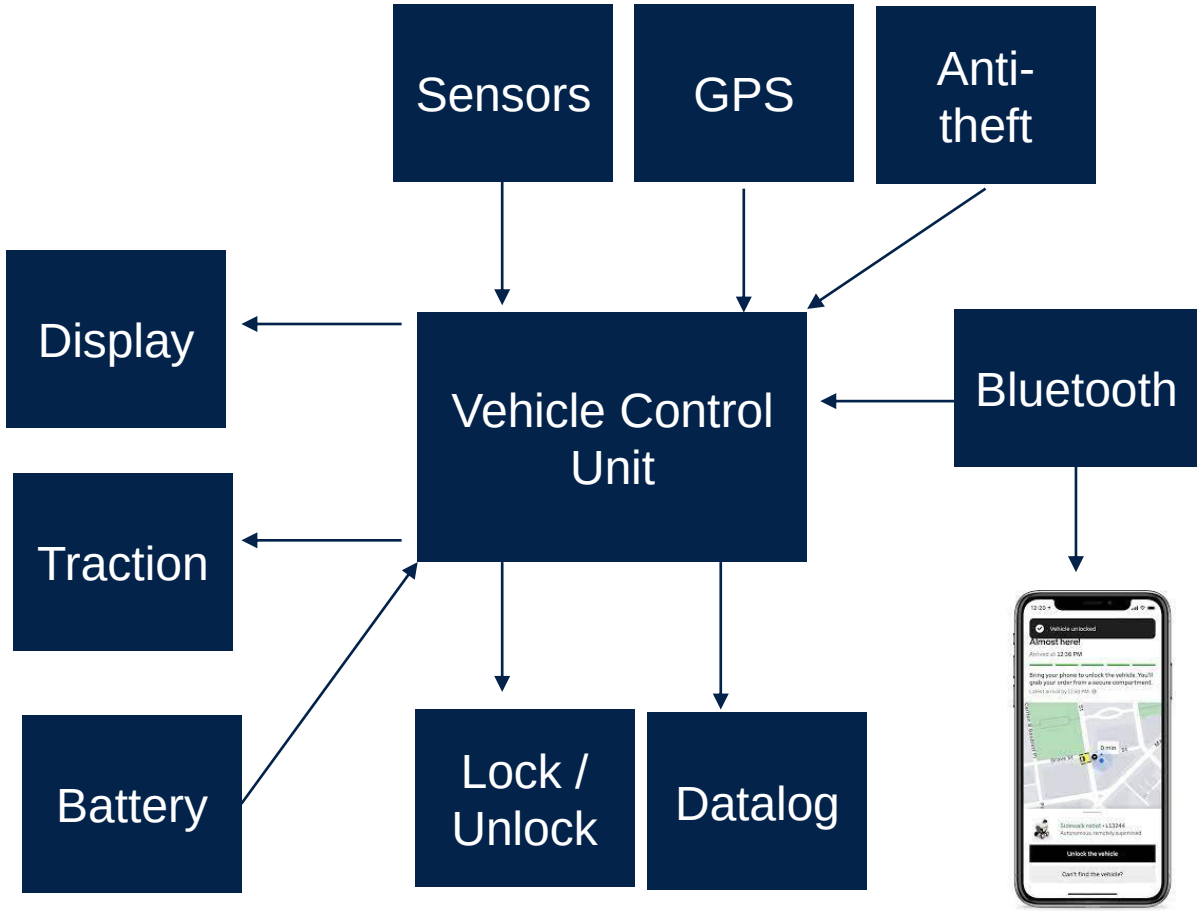
Shopping cart automatic transport

Key features:

- Small pavement vehicle
- Path finding based on map
- Hiring and releasing by APP



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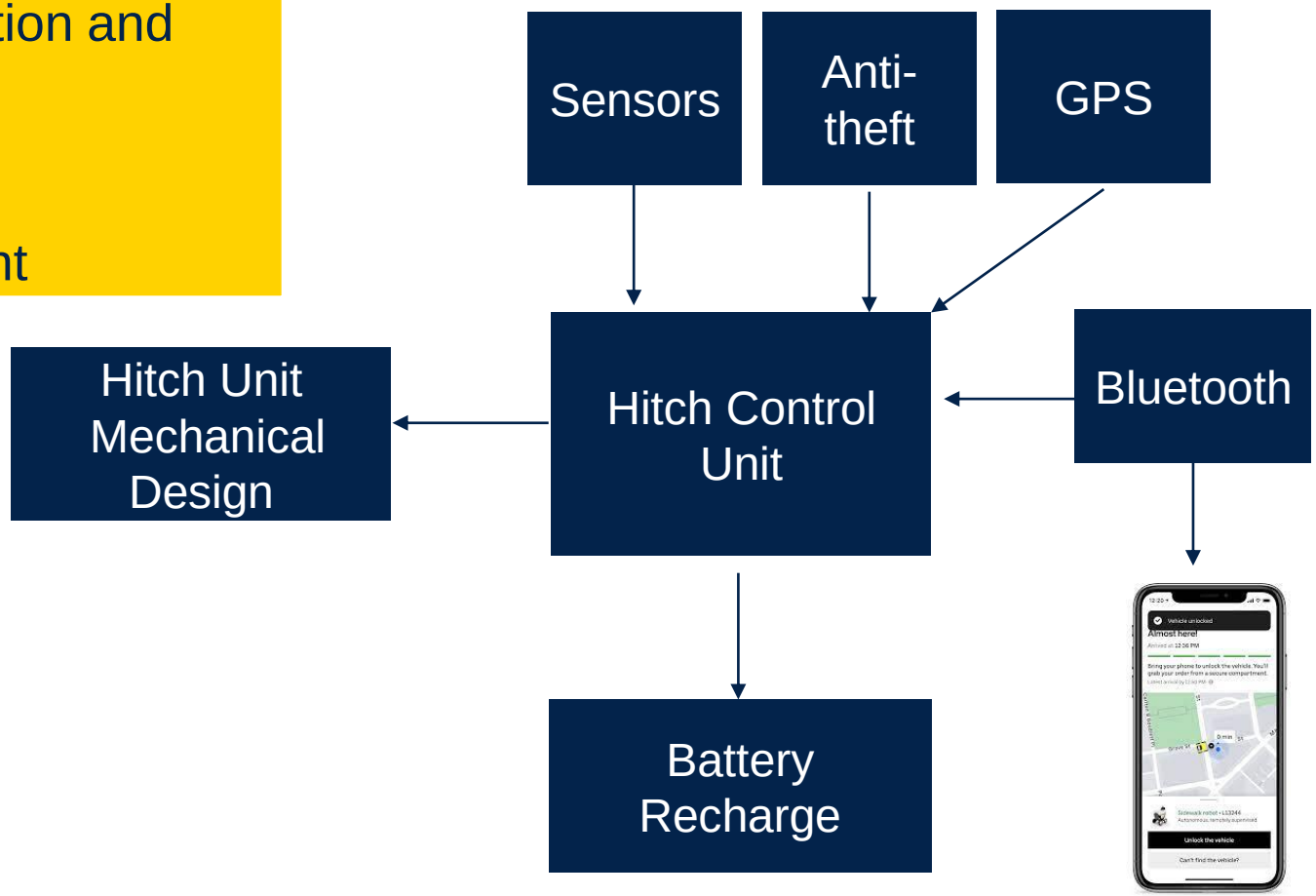
Electronic tow hitch (towed vehicle)

Key features:

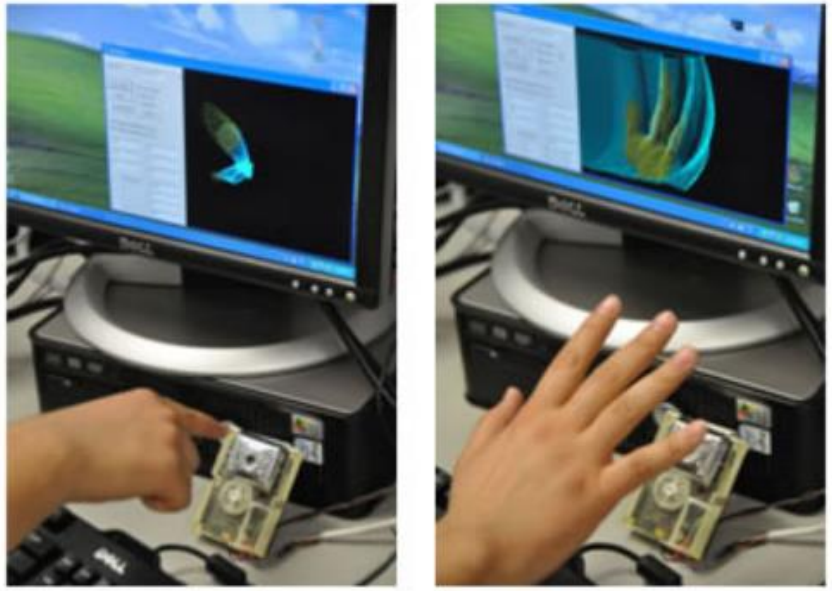
- In motion connection and disconnection
- Power delivery
- Fleet management



Touch-less in-vehicle control

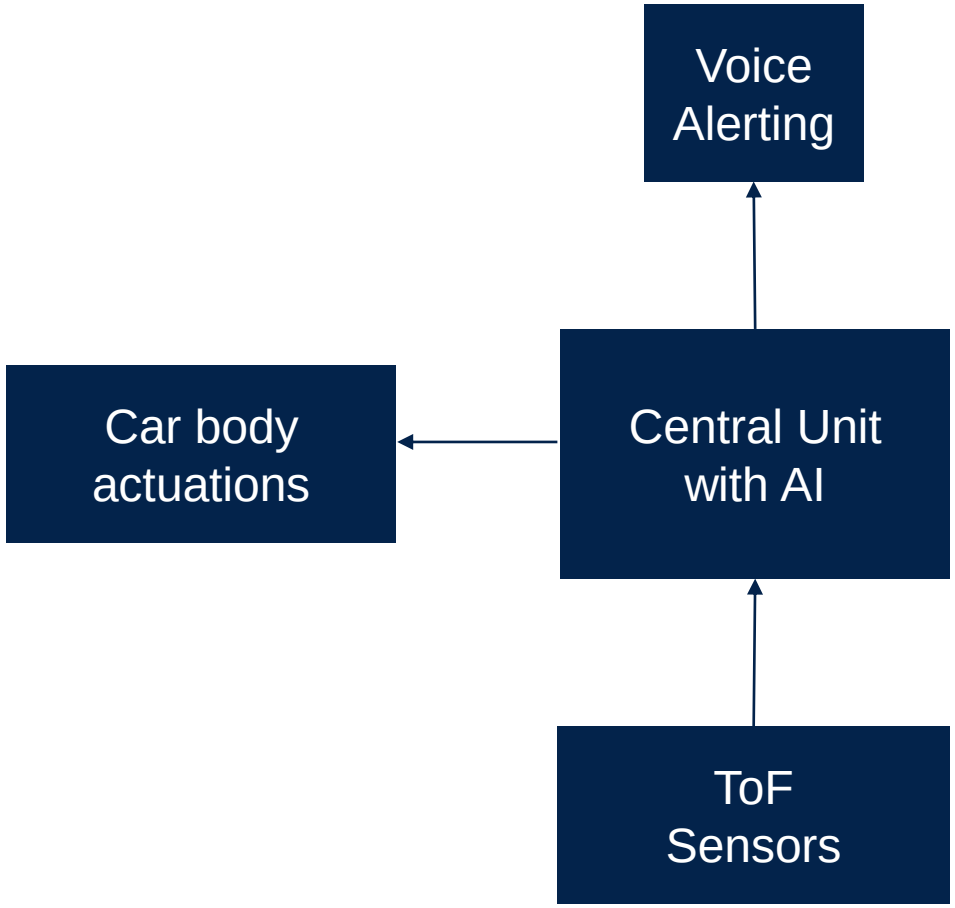
Key features:

- Based on Time-of-Flight (TOF) sensors
- Aided by machine learning
- Adaptable to several cluster controls
- Voice alerting for command confirmation



Finger input mode

Palm input mode



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Thesis Proposals - AMS

December 2022

Francesco Pappalardo
(francesco.pappalardo@st.com)

SUGGESTED STAGES & MSc FINAL PROJECTS BY STMicroelectronics

TOPICS : Digital Architecture and Design

- Design strategies definition and analysis to minimize power consumption in high-performance complex CMOS digital circuits
- Advanced architectures for best performance/power trade-off in complex ASICs targeting multiple application use cases
- Specification and Design of synchronous/asynchronous digital

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METHODOLOGY

- HDL design (VHDL, Verilog languages)
- RTL simulation CAD tools (Cadence Xcelium)
- CDC and RDC checks (Synopsys Spyglass)

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SUGGESTED STAGES & MSc FINAL PROJECTS BY STMicroelectronics

TOPICS : Front to Back

- Complete Acknowledgement of Power Simulation for Ultra-Low-Power SoC Designs.
- UPF (Unified Power Format) flow Power Assessment over Digital Design Implementation Cycle.
- CDC (Clock Domain Crossing) and RDC (Reset Domain Crossing) flow generation and integration for Post-Synthesis Netlist

METHODOLOGY

- Synthesis (Design Compile Nxt Synopsys)
- STA Static Timing Analysis (PRIME TIME Synopsys)
- Formal Verification (RTL vs netlist) (FORMALITY Synopsys)

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SUGGESTED STAGES & MSc FINAL PROJECTS BY STMicroelectronics

TOPICS : Digital Verification

- Functional Verification of Finite State Machines: an automatic UVM based approach for the verification of generic synchronous and asynchronous FSM.
- C-model based verification of a generic IP: an automatic UVM based approach for the functional verification of RTL designs through correspondence checking with a reference Cmodel.

METHODOLOGY

- System Verilog for Verification, Formal Verification
- UVM Universal Verification Methodology (VIP, Agent)
- Functional and Code Coverage with Randomized coverage driven methodology

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SUGGESTED STAGES & MSc FINAL PROJECTS BY STMicroelectronics

TOPICS : Physical Implementation

- Digital design of a custom Single-Wire Test Interface (SWTI) IP for the test time reduction of Power Management IC.
- Evaluating the power consumption impact on timing paths during ASIC physical design
- Physical design of a digital integrated circuit in BCD8 technology for AMOLED power supply application: a case study

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METHODOLOGY

- Synthesis and Place & Route CAD tools (ICC2/Fusion Compile)
- IRDrop (Redhawk Ansys)
- DRC and LVS (CALIBRE Mentor Graphics)

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Thank you

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