Eng. *Elio Consoli*, Ph.D.
Curriculum Vitae et Studiorum

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Summary of the general and main information

Elio Consoli is an **Analog & Mixed-Signal IC Design Expert** (13 years in the industry plus 3 Ph.D. years), with focus especially on **Power Management**, both as the **Leader/Architect** of complex ICs top-level design/integration/verification and as **Manager** of other designers.

In **2023** he was promoted to the role of **Senior Principal Engineer** - Analog & Mixed-Signal IC Design, having also the parallel role of **Manager** of 3 Designers and 1 Ph.D. student.

In **2021** he joined **Analog Devices** as a **Principal Engineer** - Analog & Mixed-Signal IC Design, having also the parallel role of **Manager** of 2 Designers.

In **2019** he was promoted to the role of **Principal Member of Technical Staff** - IC Design, having also the parallel role of **Supervisor** of 1 Designer.

In **2015** he was promoted to the role of **Senior Member of Technical Staff** - IC Design.

In **2013** he was promoted to the role of **Member of Technical Staff** - IC Design.

In **2011** he joined **Maxim Integrated Products** as an **Associate Member of Technical Staff** - IC Design.

In **2011** he received the **Ph.D.** in **Electronic, Automation and Control of Complex Systems Engineering** at the **University of Catania**.

In **2010** he was a **Visiting Scholar** at **Berkeley Wireless Research Center** (**BWRC**), **UC Berkeley**.

In **2008** he received the **Master's degree** (110/110 cum laude) in **Microelectronic Engineering** at the **University of Catania**.

In **2005** he received the **Bachelor's degree** in **Electronic Engineering** (110/110 cum laude) at the **University of Catania**.

Industrial activity

Products and main responsibilities

He is working / has worked in the past on many (~30) commercially successful Wearable/Healthcare, Consumer and Industrial products. In particular, he acts / acted as top-level architect or IPs developer in the design of largely complex ICs such as: PMICs, DC-DC SMPSs, Battery Chargers and Power-Paths, AC-DC Wireless Charging, Haptic (LRA/ERM Motors) Drivers, USB(-C) Interface ICs, Over-Voltage/Current Protectors, Bus Accelerators.

In addition to the main analog and mixed-signal design and managing activity, he also takes care of or supervises the following aspects:

- architecture/specs definition together with product definition and digital design teams
- behavioral modeling
- common verification environment set-up for analog/digital co-simulation
- layout guidance/supervision
- bench validation, both manual and automated
- support/guidance of automated test development
- QA verifications, datasheet reviews and products introduction under tight schedules

Technical skills

He has dealt with the design of circuits of various complexity and with high performances such as DC-DC converters (Ultra Low Power Buck / Boost / Buck-Boost, Noninverting and Inverting, SIMO, AMOLED Dual Supplies Drivers), AC-DC rectifiers, LDOs, OTAs / OPAMPs, Powertrains, Half/Full-Bridges Drivers, Charge-Pumps, Load Switches, Bandgap / Bias References, Comparators, ADCs and DACs, Analog Switches, Oscillators, PORs, Thermal Protections, High-performance Digital Circuits, High-ESD and Surge Protection Networks.

He has a strong experience in working with state-of-the-art BCD processes (180nm & 90nm), dealing with high voltage operation (e.g., 80V), low RON power FETs and with Latchup / ESD handling techniques. Cooperation with process/technology teams for the development of new flows and devices (e.g., new flavors of lateral N/P DMOS).

He is able to use the required lab equipment for bench validation and is coordinating the adoption of automated measurements platforms (e.g., NI PXI).

He has a very good experience in working with the Cadence Virtuoso Platform, Spectre/AMS simulators and OCEAN scripts to automate circuits analysis and optimization.

He has a very good knowledge of behavioral modeling languages (focus on real number modeling in Verilog-AMS and SystemVerilog plus Verilog-A) and Hardware Description Languages (VHDL and Verilog-D).

He has a very good knowledge of SIMPLIS simulator for the architectural analysis of switching DC-DC topologies.

He has knowledge of Asynchronous FSMs design approaches and tools (Workcraft).

At Ph.D. time he was involved also with full-custom layout on the Cadence Platform and with the usage of software tools for physical/design verification (Calibre), for standard-cells based synthesis of digital circuits (Design Compiler) and for PCB design and layout (Allegro

and PCB Editor). He is supervising layout / EM tools usage for automated capacitive/resistive parasitics handling, RONs / metals electrical analysis and package/PCB parasitics modeling.

Managerial skills

He has very good communication and relational skills acquired when working within large teams for the development of complex and challenging projects. He is willing to share efforts with other colleagues and direct reports with the goal of maximizing team performances.

When dealing with very complex projects, he is willing to take responsibilities in specs and functionalities definition and issues identification at top-level, which is translated in proactive collaboration and communication with business, product definition and digital-design teams.

He supervises designers both as the manager of direct reports and as a mentor for other ones, with focus on keeping them motivated to continuously improve and expand their technical background. He supervises and coordinates layout engineers, lab technicians, product/application/test engineers throughout the various phases of product development.

Relationship with the University of Catania

He proactively maintains very strong relationships with local (Faculty of Engineering, University of Catania) Electronics Professors with the joint target of increasing the local pool of students in Microelectronics, having provided many technical seminars over the years and continuously supporting internships/theses and recently also new Ph.D. programs.

Patents

Preliminary note: he started submitting patents just in 2023 since their filing was discouraged in the Maxim Integrated Products business unit where he worked in up to 2021.

1) F. Christo, E. Consoli, C. Easson, M. Di Cera, J. Georges, M. Masini, A. Mazzone, D. Melis, G. Patti, N. Prasad, Y. Yang, Y. Zhang, "Dynamic Voltage Scaling (DVS) in Photoplethysmography (PPG) Systems", US Patent, APD9780US01.
2) G. Belluco, F. Christo, E. Consoli, M. Di Cera, F. Dowling, J. Georges, M. Masini, A. Mazzone, R. Mita, G. Patti, I. Porcelli, "Power Management Devices Including Multiple Input Ports and Associated Systems and Methods", US Patent, APD9774US01.
3) G. Belluco, F. Christo, E. Consoli, M. Di Cera, J. Georges, M. Masini, A. Mazzone, D. Melis, R. Mita, G. Patti, I. Porcelli, "Current Limiting Systems and Associated Methods", US Patent, APD9879US01.
4) E. Consoli, M. Di Cera, M. Masini, G. Patti, "Single-Input Multi-Output Direct Current to Direct Current Converters and Associated Methods", US Patent, APD9891US01.
5) E. Consoli, G. Garufi, G. Patti, C. Ricca, A. Scarpata, "Full-Wave Active Rectifier Control", US Patent, APD10028US01.
6) E. Consoli, G. Patti, G. Fisichella, C. Ricca, M. Masini, M. Di Cera, "Optimal Current Pulse Shapes for SIBO DC-DC Converters", US Patent, under review.

7) E. Consoli, G. Patti, G. Fisichella, C. Ricca, "Novel Control Strategies to Handle Charge Balancing and High Load Imbalances in SIBO DC-DC Converters", US Patent, under review.

Analog Devices GTC contributions

Below is a list of contributions at the **Analog Devices** annual internal **General Technical Conference** (**GTC**).

Papers:

1) F. Christo, E. Consoli, M. Di Cera, M. Masini, G. Patti, "Dynamic Voltage Scaling and High-Efficiency Clean-Ripple Buck-Boost for PPG Applications", Boston, 2024.
2) E. Consoli, M. Di Cera, M. Masini, G. Patti, "Efficient Input Current Limited MIMO Buck-Boost with High Peak Power Capability", Boston, 2024.

Workshops:

1) P. O'Sullivan, A. Mazzone, J. Stewart, D. Simmons, E. Consoli, R. Mita, P. Wright, "Time's Up on Ad-Hoc Asynchronous State Machine Design", Boston, 2024.

Scientific activity

Research topics

His scientific research activity occurred only during the 3 years when he pursued Ph.D. (2008-2011).

The main topic was the development of novel modeling and energy-efficient design techniques for nanometer CMOS digital circuits with emphasis on clock networks and very high-speed / low-power clocked storage elements topologies.

The activity as a Visiting Scholar at BWRC (2010) was focused on the development of novel design techniques for switched-capacitor DC-DC converters and ultra low power circuits to be employed in wireless sensor networks targeting the nano-watt range of power dissipation. It culminated in the realization of a 2mm x 2mm chip prototype in ST-CMOS065 65-nm technology taped out at BWRC in April 2011 to demonstrate the above novel techniques.

Summary of the scientific production

He co-authored **1 book**, **1 book chapter**, **11** publications in **International Journals**, **20** publications in **International Conferences**.

According to SCOPUS, his **h-index** is **12**.

Publications list

Books:

1) M. Alioto, E. Consoli, G. Palumbo, "Flip-flop Design in Nanometer CMOS: From High Speed to Low Energy", Springer, August 2016.

Books chapters:

1) M. Alioto, E. Consoli, G. Palumbo, "Design in the Energy-Delay Space," in Advanced Circuits for Emerging Technologies, Part I - Digital Design and Power Management, 1st Chapter, Wiley, June 2012.

International Journals:

1) M. Alioto, E. Consoli, G. Palumbo, "General Strategies to Design Nanometer Flip-Flops in the Energy-Delay Space," IEEE Transactions on Circuits and Systems – Part I, vol. 57, no. 6, pp. 1273-1286, June 2010.
2) M. Alioto, E. Consoli, G. Palumbo, "Flip-Flop Energy/Performance versus Clock Slope and Impact on the Clock Network Design," IEEE Transactions on Circuits and Systems – Part I, vol. 57, no. 7, pp. 1583-1596, July 2010.

3) M. Alioto, E. Consoli, G. Palumbo, "Analysis and Comparison in the Energy-Delay-Area Domain of Nanometer CMOS Flip-Flops: Part I - Methodology and Design Strategies," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 19, no. 5, pp. 725-736, May 2011.
4) M. Alioto, E. Consoli, G. Palumbo, "Analysis and Comparison in the Energy-Delay-Area Domain of Nanometer CMOS Flip-Flops: Part II – Results and Figures of Merit," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 19, no. 5, pp. 737-750, May 2011.
5) E. Consoli, G. Giustolisi, G. Palumbo, "An Accurate Ultra-Compact I-V Model for Nanometer MOS Transistors with Applications on Digital Circuits," IEEE Transactions on Circuits and Systems – Part I, vol. 59, no. 1, pp. 159-169, January 2012.
6) E. Consoli, G. Palumbo, M. Pennisi, "Reconsidering High-Speed Design Criteria for Transmission-Gate Based Master-Slave Flip Flops," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 20, no. 2, pp. 284-295, February 2012.
7) M. Alioto, E. Consoli, G. Palumbo, "From Energy-Delay Metrics to Constraints on the Design of Digital Circuits," International Journal of Circuit Theory and Applications, vol. 40, no. 8, pp. 815-834, August 2012.
8) M. Alioto, E. Consoli, J. Rabaey, ""EChO" Reconfigurable Power Management Unit for Energy Reduction in Sleep-Active Transitions," IEEE Journal of Solid-State Circuits, vol. 48, no. 8, pp. 1921-1932, August 2013.
9) E. Consoli, G. Palumbo, J. Rabaey, M. Alioto, "A Novel Class of Energy-Efficient Very High-Speed Conditional Push-Pull Pulsed Latches," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 22, no. 7, pp. 1593-1605, July 2014.
10) M. Alioto, E. Consoli, G. Palumbo, "Variations in Nanometer CMOS Flip-Flops: Part I – Impact of Process Variations on Timing," IEEE Transactions on Circuits and Systems – Part I, vol. 62, no. 8, pp. 2035-2043, August 2015.
11) M. Alioto, E. Consoli, G. Palumbo, "Variations in Nanometer CMOS Flip-Flops: Part II – Energy Variability and Impact of Other Sources of Variations," IEEE Transactions on Circuits and Systems – Part I, vol. 62, no. 3, pp. 835-843, March 2015.

International Conferences Proceedings:

1) M. Alioto, E. Consoli, G. Palumbo, "Metrics and Design Considerations on the Energy-Delay Tradeoff of Digital Circuits," in Proc. of ISCAS, pp. 3150-3153, May 2009.
2) M. Alioto, E. Consoli, G. Palumbo, "Impact of Clock Slope on Energy/Delay of Pulsed Flip-Flops and Optimum Clock Domain Design," in Proc. of ECCTD, pp. 61-64, August 2009.
3) M. Alioto, E. Consoli, G. Palumbo, M. Pennisi, "Correct Procedures to Evaluate the Effect of Intradie Variations on the Delay Variability of Digital Circuits," in Proc. of ECCTD, pp. 779-782, August 2009.
4) M. Alioto, E. Consoli, G. Palumbo, "Dependence of Differential Flip-Flops Performance on Clock Slope and Relaxation of Clock Network Design," in Proc. of ICM, pp. 110-113, December 2009.
5) M. Alioto, E. Consoli, G. Palumbo, "Optimum Clock Slope for Flip-Flops within a Clock Domain: Analysis and a Case Study," in Proc. of ICECS, pp. 275-278, December 2009.

6) M. Alioto, E. Consoli, G. Palumbo, "Clock Distribution in Clock Domains with Dual-Edge Triggered Flip-Flops to Improve Energy-Efficiency," in Proc. of ISCAS, pp. 321-324, June 2010.
7) M. Alioto, E. Consoli, G. Palumbo, "Physical Design Aware Comparison of Flip-Flops for High-Speed Energy-Efficient VLSI Circuits," in Proc. of PATMOS, pp. 62-72, September 2010.
8) M. Alioto, E. Consoli, G. Palumbo, "Physical Design Aware Selection of Energy-Efficient and Low-Energy Nanometer Flip-Flops," in Proc. of ICM, pp. 60-63, December 2010.
9) M. Alioto, E. Consoli, G. Palumbo, "Nanometer Flip-Flops Design in the E-D Space," in Proc. of ICM, pp. 132-135, December 2010.
10) M. Alioto, E. Consoli, G. Palumbo, "DET FF Topologies: A Detailed Investigation in the Energy-Delay-Area Domain," in Proc. of ISCAS, pp. 563-566, May 2011.
11) E. Consoli, G. Palumbo, M. Pennisi, "TG Master-Slave FFs: High-Speed Optimization," in Proc. of ISCAS, pp. 554-557, May 2011.
12) E. Consoli, G. Giustolisi, G. Palumbo, "An Ultra-Compact MOS Model in Nanometer Technologies," in Proc. of ECCTD, pp. 520-523, August 2011.
13) E. Consoli, G. Giustolisi, G. Palumbo, "Inverter Transfer Curves and SRAM Noise Margin Evaluation Based on an Ultra-Compact MOS Model," in Proc. of ECCTD, pp. 512-515, August 2011.
14) E. Consoli, M. Alioto, G. Palumbo, J. Rabaey, "Conditional Push-Pull Pulsed Latches with 726fJ•ps Energy-Delay Product in 65nm CMOS," in Proc. of ISSCC, pp. 9-11, February 2012.
15) E. Consoli, G. Giustolisi, G. Palumbo, "Logic Gates Dynamic Modeling by Means of an Ultra-Compact MOS Model," in Proc. of ISCAS, pp. 3250-3253, May 2012.
16) M. Alioto, E. Consoli, J. Rabaey, "EChO Power Management Unit with Reconfigurable Switched-Capacitor Converter in 65 nm CMOS," in Proc. of CICC, pp. 1-4, September 2012.
17) M. Alioto, E. Consoli, G. Palumbo, "Analysis and Comparison of Variations in Double Edge Triggered Flip-Flops," in Proc. of VARI, pp. 1-6, September 2014.
18) M. Alioto, G. Palumbo, E. Consoli, "Variability Budget in Pulsed Flip-Flops," in Proc. of NEWCAS, pp. 1-4, June 2015.
19) M. Alioto, G. Palumbo, E. Consoli, "PVT Variations in Differential Flip-Flops: A Comparative Analysis," in Proc. of ECCTD, pp. 1-4, August 2015.
20) M. Alioto, E. Consoli, G. Palumbo, "Comparative Analysis of the Robustness of Master-Slave Flip-Flops against Variations," in Proc. of ICECS, pp. 117-120, December 2015.

Il sottoscritto dichiara che il presente CV è redatto ai sensi degli artt. 46 e 47 del DPR n° 445 del 28.12.2000.

Gravina di Catania, 13rd September 2024 Elio Consoli