

Prof. *Gaetano Palumbo*, PhD
Curriculum Vitae

DIEEI

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Summary of the general and main information

Gaetano Palumbo, was born in Catania, Italy, on 11 September 1964, his **h-index** according to SCOPUS is equal to **47** and his papers have received more than **8300** citations. Since the 2017 he has been in the Stanford ranking of the 2% best scientists (for the career and since 2019 also in each year ranking).

Since **2026** he is in the **board** of **CHIP4POWER** consortium established by the Chips JU to build the integrated Pilot Line focused on the development of wide-bandgap (WBG) semiconductor technologies for power and radio frequency electronics.

Since **2022** he is serving as **Editor in Chief** of the open access journal *Chips* (the former of the journal), which in 2025 become indexed by SCOPUS.

Since **2019** he is serving in the **Editorial Board** of the open access journal *Electronics*.

Since **2018** to **2020**, he served as the **Vice-Chair** of association *SIE (Società Italiana di Eletttronica)*.

In **2016** he was the **Chair** of the *IEEE CASS Committee* for evaluation of the *Fellow Nomination*.

In **2015** he was a **panelist** of **GEV** (Group of Evaluation Expert) in the **scientific area 09 - industrial and information engineering** of the ANVUR for **VQR** (Evaluation of Italian Research Quality) **2011-2014**, which has the aim to evaluate the Italian research in the above area for this time interval.

Since **2014** to **2021** he was in the **board** of association *GE (Gruppo Italiano di Eletttronica)*, now named *SIE (Società Italiana di Eletttronica)*. In particular, he was elected the first time for the period 2014-2017 and then re-elected for the period 2018-2021 was appointed Vice Chair.

In 2010 he was elected for the period **2011-2013 member** of the **Board of Governors** of IEEE Circuits and Systems Society.

At the end of 2008 he was one of the proponent and member of the **University Spin-off MicroSensor srl.**, and since the **2009** up to **2014** he was also the **CEO**.

Since January **2008** to December **2011** he served as **Associated Editor** of *IEEE Transactions on Circuits and Systems - part I* (he was in the editorial board of 2008-2009 and now is in the one of 2010-2011).

Since **2007** he is a **Fellow IEEE** with the following citation: “*For contributions to analysis and design of high performance analog and digital circuits*”.

Since **2006** to **2012** he was on the board of the **Nucleo di Valutazione** (i.e., evaluation panel) of the University of Catania.

Since January **2006** to the end of **2007** he served as **Associated Editor** of *IEEE Transactions on Circuits and Systems - part II*, and for this activity he was recognized among **the best 5** Associate Editors of the editorial board.

In **2005** he was a **panelist** (of 12) in the **scientific-disciplinare area 09 - industrial and information engineering** of the **CIVR** (Committee for Evaluation of Italian Research), which has the aim to evaluate the Italian research in the above area for the period 2001-2003 .

From January **2004** to December **2005** he served as **Associated Editor** of *IEEE Transactions on Circuits and Systems (part I)* topic: digital circuits and systems.

In **2003** he received the **Darlington Award** (Purpose: To recognize the best paper bridging the gap between theory and practice published in *IEEE Trans. on CAS Part I* or *Part II*, during the two calendar years preceding the award) for the paper “Charge Pump Circuits: Power Consumption Optimization”, *IEEE Trans. on CAS part I*, Vol. 49, No. 11, Nov. 2002.

Since **2000** he is a **Full Professor** of Electronics (Italiana SSD IINF-01/A Elettronica), at the University of Catania.

From July **1999** to December **2001** he served as **Associated Editor** of *IEEE Transactions on Circuits and Systems (part I)* topic: analog circuits and signal processing.

Since **1998** he is a *IEEE Senior Member*.

In **1998** he became **Associated Professor** of Electronics (Italian SSD ING-INF/01)

In **1993** he joined the Department of Electrical Electronics and System (DEES) at the University of Catania as an **Assistant Professor**.

In **1993** he got through the final Ph.D. in Electrical Science.

In **1989** he started the Ph.D. in Electrical Engineering. The same year he was awarded with a grant by AEI of Catania.

In **1988** he received the Laurea degree in Electrical Engineering at the University of Catania.

Teaching activities

Since the academic year **2020-2021** he has been teaching a module of the course “*Electron device*” (4 cr.) for the First level Laurea Degree of Electronics Engineering at the University of Catania.

Since the academic year **10-11** he has been teaching “*Digital Electronics*” (10 cr.), and since **04-05** to **09-10** and since **05-06** to **10-11** he taught “*Digital Circuits and Microelectronics laboratory*” (6 cr. + 3 cr.) and “*VLSI Systems*” (6. cr), respectively, all for the Second level Laurea Degree (laurea specialistica/magistrale) on Microelectronics Engineering, at the University of Catania. Moreover, in the academic year **03-04** and **04-05** he taught “*Digital Electronics*” (6 cr.) for the First level Laurea Degree on Electronics Engineering, at the same university.

In **2000** he was the *chairman* of a didactic agreement between DEES and STmicroelectronics, and according to it, he gave several courses on *CMOS VLSI*.

In **1999** and **2000** he was *organizer* and *teacher* of some parts of the “*Master of Microelectronics and Systems*” and the “*Advanced course in Microelectronics and Systems*” for the topics “CAD” and “Design of VLSI systems and related CAD”, respectively, both organized by the Catania High School.

In the academic years **1999-2000** and **1993-1994** he conducted a course on “*Electronic Devices*” in the “Diploma in Ingegneria Elettronica” at the Università di Catania.

In the academic years **1998-1999** to **2002-2003** he taught “*Electronics (first course)*” for both the Informatic Engineering and Electric Engineering Laurea degrees, at the University of Catania.

Since **1998** to **2000** he was a teaching staff member for the Ph.D. in “*Electrical Engineering*” at the University of Catania, and since **2001** at present he is a teaching staff member for the Ph.D. in “*Electronics and Automation Engineering*” at the University of Catania.

Since the academic year **1997-1998** to **2003-2004** he taught “*Electronics for digital systems*” for both the Electronics Engineering and the Informatic Engineering Laurea degrees at the University of Catania.

In **1996** he was *designer* and *coordinator* of the course “Tecnico CAD-CAE di Schede Elettroniche” cofounded by “European social found” and “Fondo di Rotazione del Ministero del Lavoro”.

He was tutor of 11 Ph.D. students and at the present he is the tutor of other three, all in the area of microelectronics. Moreover, he was the tutor of more than 170 Laurea degree thesis.

Scientific activity

Research Topics

His main field of research is *electronic circuits* with emphasis on *microelectronics*.

He started his researches with the laurea degree thesis working on the application of artificial intelligence to the design of analog circuits. Then, about two years later, he began investigation in the design and modeling of analog circuits both in the continuous and discrete time, including nonlinear circuits such as neural networks and Fuzzy systems.

His main results in the analog circuit domain were found on:

- analog current-mode circuits;
- charge pump;
- non linear circuits (mainly devote to fuzzy systems);
- integrated analog filters;
- optimized frequency compensation techniques;
- analysis and design of amplifier and analog circuits;
- low-voltage circuits;
- voltage references and regulators;
- oscillators;
- techniques to analyze harmonic distortion;
- interface for single photon sensors.

His research embraced also digital circuits with emphasis on high performance digital circuit in term of high speed or low power. In particular, main results were found on the below topics:

- bipolar and MOS current mode logic: CML, ECL and SCL (or MCML);
- adiabatic circuits;
- digital systems for industrial and domestic communication;
- pseudorandom number generators;
- circuits for non volatile memories (sense amplifier, buffer, etc.);
- systems and circuits for adders;
- interconnections modelling;
- performance variations on digital circuits due to power supply variation;
- performance variations on digital circuits due process mismatches;
- analysis and design of sequential circuits;
- design strategies of digital circuit by using nanometric technologies.

Summary of the scientific production

Gaetano Palumbo is the co-author of the **6 books**, 5 of which: “*CMOS Current Amplifiers*”, “*Feedback Amplifiers: Analysis and Design*”, “*Model and Design of Bipolar and MOS Current-Mode Logic (CML, ECL and SCL Digital Circuits)*”, “*Flip-Flop Design in Nanometer CMOS (High Speed to Low Energy)*”, “*High-Performance Integrated Charge Pumps (Design and Novel Solutions)*” published with Kluwer Academic Publishers and Springer in 1999, 2002, 2005, 2014 and 2023, respectively; one is the textbook on electron devices “*Introduzione ai Dispositivi Elettronici*” published with Franco Angeli in 2005, which is now the textbook of Electron Device not only at the university of Catania but also at the Milan Polytechnique. Moreover, he is the author of a chapter on *Enciclopedia of Electrical and Electronics Engineering*, published by Wiley.

He is author or co-author of more than **470 paper**, about **220 on referred international journals**, and about **250 papers on international conferences** and several papers on national journal.

He also hold **6 patents**, and reviewed several books for international journal.

According to SCOPUS, the **h-index** of Gaetano Palumbo is **47** and his scientific papers, published on the international scientific journals shown in Table I, have received more than **8300 citations**.

Since the 2017 he has been in the Stanford ranking of the 2% best scientists (for the career and since 2019 also in each year ranking).

Table I

Journal	N.
IEEE Trans. on Circuits and Systems (part I and part II)	84
IEEE Journal of Solid-State Circuits	5
IEEE Trans. on Power Electronics	2
IEEE Trans. on Instrumentations and Measurements	4
IEEE Trans. on CAD	1
IEEE Trans. on VLSI	13
IEEE Access (open source)	9
IEEE Trans. on Education	1
IEEE Trans. on Fuzzy Systems	1
IEEE Journal of Display Technology	1
IEEE Sensors Journal	1
IEEE Circuits and Systems Magazine	3
Electronics Letters	18
Intern. Journal of Circuit Theory and Applications	35
Proc. IEE part G (Circuits, Devices and Systems) now IET	10
Analog Integrated Circuits and Signal Processing	12
Microelectronica Journal	7
Integration – The VLSI Journal	3
Journal of Low Power Electronics and Appl. (JLPEA) (open source)	3
Electronics (open source)	8
Other	11

Awards

Since **2007** he is a **Fellow IEEE** with the following citation: “*For contributions to analysis and design of high performance analog and digital circuits*”.

In **2007** was awarded as one of the **5 best Associate Editors** serving during 2006-2007 the *IEEE Transactions on Circuits and Systems - part II* editorial board.

In **2003** he received the **Darlington Award** (Purpose: To recognize the best paper bridging the gap between theory and practice published in *IEEE Trans. on CAS Part I or Part II*, during the two calendar years preceding the award) for the paper “Charge Pump Circuits: Power Consumption Optimization”, *IEEE Trans. on CAS part I*, Vol. 49, No. 11, pp. 1535-1542, November 2002.

In **1999** he received the **Outstanding Paper Award** at the conference MIXDES’99 (Mixed Design of Integrated Circuits and systems), held in Krakow, for paper “Noise Performance Of Current-Feedback Operational Amplifiers” (authors: G. Palumbo and S. Pennisi).

Editorial and scientific boards or committees

In **2025** **Guest Editor** of *IEEE Transactions on Circuits and Systems - part II* for Special Issue on ISICAS 2025.

In **2025** **member** of the committee for the *IEEE CASS Mac Van Valkenburg Award Nominations*.

Since **2022** he is serving as **Editor in Chief** of the open access journal *Chips* (the former of the journal), which in 2025 become indexed by SCOPUS.

In **2022-2025** **Special Issue Editor** of "Ultra-Low-Voltage and Ultra-Low-Power Integrated Circuits and Systems Evolution", of the open access journal *Electronics*.

In **2021-2024** **Special Issue Editor** of "Feature Papers in Circuit and Signal Processing", of the open access journal *Electronics*.

Since **2019** he is serving in the **Editorial Board** of the open access journal *Electronics*.

In **2018** he was the **Tutorial co-Chair** of the *IEEE ISCAS 2018 Conferences*.

In **2017** he was the **General co-Chair** of the *IEEE PRIME 2017 Conferences*.

In **2016** he is the **Chair** of the *IEEE CASS Committee* for evaluation of the *Fellow Nomination*.

In **2015** he has been a **panelist** of **GEV** (Group of Evaluation Expert) in the **scientific area 09 - industrial and information engineering** of the ANVUR for **VQR** (Evaluation of Italian Research Quality) **2011-2014**, which has the aim to evaluate the Italian research in the above area for this time interval.

In 2010 he was the only European to be elected for the period **2011-2013 member** of the **Board of Governors** of IEEE Circuits and Systems Society.

In **2010** and **2011** he was a **member** of *IEEE CASS Committee* for evaluation of the *Fellow Nomination*.

In **2008** he was a **member** of *IEEE CASS Meritorious Service Award* committee.

Since January **2008** to December **2011** he served as **Associated Editor** of *IEEE Transactions on Circuits and Systems - part I* (he was in the editorial board of 2008-2009 and 2010-2011).

Since January **2006** to the end of **2007** he served as **Associated Editor** of *IEEE Transactions on Circuits and Systems - part II*, and for this activity he was recognized among **the best 5** Associate Editors of the editorial board.

In **2005** he was one of the 12 **panelists** in the **scientific-disciplinary area 09 - industrial and information engineering** of the **CIVR** (Committee for Evaluation of Italian Research), which has the aim to evaluate the Italian research in the above area for the period 2001-2003.

Since January **2004** to the end of **2005** he served as **Associated Editor** of *IEEE Transactions on Circuits and Systems - part I*, topic: digital circuits and systems.

Since **2003** he is a member of **VLSI systems and applications Technical Committee** of the IEEE Circuits and Systems Society.

Since **2002** he is a member of **Analog Signal Processing Technical Committee** of the IEEE Circuits and Systems Society.

From July **1999** to December **2001** he served as **Associated Editor** of *IEEE Transactions on Circuits and Systems (part I)* topic: analog circuits and signal processing.

Since 2002 he was in the *Review Committee* of the ISCAS.

Moreover, he was also in

- *Technical Program Committee* of LASCAS 2027, Panama City, Panama.
- *Technical Program Committee* of ICECS 2026, Thessalonik, Greece
- *Technical Program Committee* of LASCAS 2026, Arequipa, Perú.
- *Technical Program Committee* of PRIME 2026, Berlin, Germany.
- *Technical Program Committee* of PRIME 2025, Taormina, Italy.
- *Award e Local Committee* of DCIS 2024, Catania, Italy .
- *Technical Program Committee* of VLSI-SoC 2023, Dubai, United Arab Emirates.
- *Technical Program Committee* of ICECS 2019, Genoa, Italy.
- *Technical Program Committee* of PRIME 2019, Lausanne, Switzerland.

- *Technical Program Committee of ICECS 2018*, Bordeaux, France.
- *Program Committee of ECCTD 2015*, Trondheim, Norway.
- *Technical Program Committee of PRIME 2013*, Villach, Austria.
- *Technical Program Committee of ECCTD 2011*, Linköping, Sweden.
- *Technical Program Committee of WISES 10*, Crete, Greece.
- *Technical Program Committee of WISES 09*, Ancona, Italy.
- *Scientific Committee of ECCTD 2009*, Antalya, Turkey.
- *Scientific Committee of ECCTD 2007*, Seville, Spain.
- *Technical Committee of PRIME 2007*, July 2007, Bordeaux, France.
- *Technical Committee of PRIME 2006*, June 2006, Otranto, Italy.
- *Scientific Committee of ECCTD 2005*, Settembre 2005, Cork, Ireland.
- *Technical Committee of ACM'02* (Algerian Conference Microelectronics), October 2002, El Aurassi Algiers, Algeria.
- *Steering Committee of ELECO'2003* (International Conference of Electrical and Electronics Engineering), December 2003, Bursa, Turkey.

He served as reviewer of several papers (over 250) for the following international journal :

- *IEEE Trans. on Circuits and System part I*;
- *IEEE Trans. on Circuits and System part II*;
- *IEEE Journal of Solid State Circuits*;
- *IEEE Trans. On Electron Devices*,
- *Electronics Letters*;
- *IEE Proceedings – Circuits, Devices and Systems (now IET)*;
- *Analog Integrated Circuits and Signal Processing*;
- *Microelectronics Journal*;
- *Journal of Circuits, Systems and Signal Processing*;
- *ETRI Journal*.

and for conferences such as: ISCAS, ECCTD e ICECS (in these conferences he was chairman several times).

Industrial research and collaborations

Since 2022 he is **scientific responsible** of the topic “Smart Mobility” (one of the seven pillar of the project) of the SAMOTHRACE (Sicilian Micro and Nano Technology Research and Innovation Center) project supported by PNNR (Piano Nazionale di Ripresa e Resilienza), project code ECS00000022. In the same project, for the Spoke 1 (which refer to teh activity of the Catania University he is also **WP leader** for the same topic.

Since 2009 up to 2013 he was **responsible** of the research: “*Sensoristica Innovativa basata su Microdispositivi Ottici?*” (Novel sensor based on Optics Microdevices), for an amount of **770.000 €** carried out by Microsensor srl and supported for 550.000 euro by Italian Minister MIUR (ministero dell’Istruzione dell’Universita e della Ricerca).

Since 2005 he was responsible of a scientific agreement between the DIEES and the MPG group of STmicroelectronics (Catania site), two years long, on the topic “*Development and characterization of memories in advanced technologies* (Supporto per lo sviluppo e la caratterizzazione di memorie in tecnologie avanzate)”

Both in 2003 and in 2000 he was scientific agreement’s responsible between the DIEES and the MPG group of STmicroelectronics (Catania site), one year long, on the topic “*Development and characterization of memories in advanced technologies* (Supporto per lo sviluppo e la caratterizzazione di memorie in tecnologie avanzate)”, and in 2003 he also is scientific agreement’s responsible between the DIEES and the DSG group of STmicroelectronics (Catania site), one year long, on the topic “*Development of digital and analog circuits using high-performance technologies both bipolar (HSB4) and BiCMOS on isulator (DIB)* (Sviluppo di circuiti digitali ed analogici con tecnologie ad elevate prestazioni sia bipolari (HSB4) che BiCMOS isolata dielettricamente (DIB))”. Moreover, in 1999 he took part of a scientific agreement research between the DEES and the Soft Computing group of ST-microelectronics, on the topic “Novel solution to implement CNN”. Nevertheless, outside these two scientific agreement, he developed research activities in collaboration with ST microelectronics (Catania site), including TPA group.

In 2000 he was also responsible of a scientific agreement between the DEES and the Tecnos Media Srl, inside the project “IR wirelss systems (Sistemi wireless a IR)” N° 214, co-financed by founds POP 1994-1999 (point 3.3B).

He took part to several European and national researches. In particular, the European project was ESPRIT *I-SMILE* part I and part II, in 1992 and 1993, respectively, and the Italian research Promaetheus-Prochip, and many 40% researches.

Scientific works' road map

- Circuit design by using AI ([c1-c4], [I1-I2], [I4-I5])
- Neural network and Fuzzy circuits ([j1], [j41], [j52], [j61], [j64], [c5-c8], [c32], [c60], [c64], [c70], [c73], [c91], [c126], [c130], [c133], [I6])
- Power integrated circuits, Smart Power and industrial circuits
 - Charge pump Voltage booster and* ([b6], [j2-j3], [j10-j11], [j20-j21], [j42], [j71], [j97], [j101], [j140], [j180]-[j181], [j183], [j185], [j187], [j189]-[j193], [j199], [j204], [j210], [j212], [j214], [j216]-[j217], [j222], [j224], [c9-c10], [c12], [c16], [c20], [c28], [c80], [c105], [c241], [c243]-[c244], [c247]-[c252], [c259])
 - Fundamental building blocks* ([j18], [c13], [c22], [c65])
 - Integrated DC-DC converter* ([c255])
- Discrete time circuits ([j5], [j7], [c14], [c18], [I7])
- Current-mode approach ([b1])
 - Current Schmitt Triggers* ([j13], [j28], [c11], [c15])
 - Current mirrors* ([j4], [j6], [j19], [c17], [c21], [c42], [I9])
 - Current comparator* ([j8-j9], [j12], [j22], [c19], [c23], [c27], [c100])
 - Current Conveyor* ([j17], [j32], [j55], [j207], [j221], [j228], [c24-c25], [c29], [c54], [c68], [c74], [c108], [c254], [c260], [c262], [I8])
 - Current Amplifiers* ([j15], [j25-j26], [j38], [j51], [j163], [c31], [c34], [c36], [c45], [c48], [c66-c67], [c224])
 - Current Feedback Amplifiers* ([j36], [j44], [j56], [j85], [j89], [j92], [c40-c41], [c57-c59], [c99], [c115])
- Amplifiers
 - Analysis and design of amplifiers* ([b2-b3], [j29-j31], [j34], [j42], [j46], [j57], [j59], [j81], [j115], [j116], [j129], [j141]-[j143], [j149], [j152], [j161], [j173], [j179], [j184], [j195], [j197]-[j198], [j201], [j205]-[j206], [j209], [c33], [c38-c39], [c43], [c53], [c56], [c94], [c96], [c98], [c136], [c163], [c168], [c170], [c192], [c198], [c205]-[c206], [c210], [c214], [c231], [c236]-[c237], [c240], [c246])
 - Compensation techniques* ([j14], [j23], [j37], [j63], [j79], [j108], [j117], [j120], [j122], [j126], [j131], [j133], [j139], [j147]-[j148], [j159], [j168]-[j174], [j176], [j178], [j195], [j208], [c26], [c30], [c50], [c69], [c78], [c94], [c98], [c120], [c155], [c160], [c171], [c178], [c193], [c199], [c204], [c221], [c225], [c230], [c234], [c235])
 - Distortion Analysis* ([j27], [j76], [j83], [j95], [j99], [j102], [j104], [j121], [j128], [j132], [j136], [c88], [c93], [c117], [c122], [c123], [c127], [c139], [c144], [c158], [c161], [c164], [c176]-[c177], [c189], [c197])
- Low-voltage circuits ([j16], [j24], [j33], [j35], [j38], [j45], [j47], [j49], [j70], [j73], [j77], [j84], [j91], [j93], [j134], [j138], [j147], [j167], [j180], [j182], [j201], [j205], [j209], [j219]-[j220], [j223], [j225], [c37], [c44], [c47], [c49], [c52], [c107], [c113]-[c114], [c118], [c119], [c128], [c165], [c175], [c185], [c231], [c251], [c256]-[c258])
- Circuits and models for single photon sensors ([j107], [j124]-[j125], [j157], [j164], [j203], [c143], [c145], [c150], [c213], [c220], [c223], [c226], [c228], [c233])

- Other topics in analog circuits ([j54], [j68], [j75], [j94], [j105], [j110], [j127], [j177], [j227], [c35], [c76], [c97], [c134], [c140], [c142], [I10])
- Current mode logic
 - CML and ECL* ([b4], [j39-j40], [j48], [j53], [j60], [j82], [j86], [j96], [j98], [j100], [c46], [c51], [c55], [c71], [c81], [c101], [c106], [c126], [c137], [c141], [c159], [I12])
 - SCL (or MCML)* ([b4], [j53], [j62], [j80], [j90], [j109], [j111], [j123], [j175], [j186], [j188], [j194], [j196], [j200], [j202], [J218], [c87], [c89], [c92], [c110], [c116], [c138], [c156], [c169], [c183], [c238], [c242], [c246])
- Adiabatic logic circuits ([j50], [j58], [j65], [c62], [c72], [c77], [I11])
- Systems and circuits for adders ([j72], [j74], [j112-j113], [j119], [j151], [j211], [j215], [c63], [c86], [c125], [c129], [c154], [c166], [c172], [c174], [c181])
- Nonvolatile memories ([j67], [c83], [c84], [c85], [c104], [c132], [c162], [I14])
- Pseudorandom number generators ([j66], [j106], [j213], [c102], [c121], [c124])
- Interconnections modeling ([j78], [j87], [j103], [j114], [j135], [j137], [c103], [c111], [c131], [c146], [c167], [c179]-[c180], [c182], [c185], [c188])
- Sequential circuits ([b8], [j145-j146], [j153-j154], [j156], [j162], [j165-j166], [c187], [c195], [c201]-[c203], [c207]-[c209], [c211]-[c212], [c217], [c222], [c227], [c229], [c232])
- Other topics in digital domain ([j69], [j118], [j130], [j144], [j150], [j155], [j158], [J160], [J226], [c61], [c75], [c82], [c90], [c95], [c109], [c157], [c173], [c186], [c190]-[c191], [c194], [c196], [c200], [c215]-[c216], [c218]-[c219], [c261], [I13])

Scientific papers full list

Books and books' chapters

- [b1] **G. Palmisano, G. Palumbo, S. Pennisi**, *CMOS Current Amplifiers*, Kluwer Academic Publisher, February 1999.
- [b2] **G. Palumbo, S. Pennisi**, "Signal Amplifiers," *Enciclopedia of Electrical and Electronics Engineering*, Wiley, 1999.
- [b3] **G. Palumbo, S. Pennisi**, *Feedback Amplifiers: Theory and Design*, Kluwer Academic Publisher, January 2002.
- [b4] **M. Alioto, G. Palumbo**, *Model and Design of Bipolar and MOS Current-Mode Logic (CML, ECL and SCL Digital Circuits)*, Kluwer Academic Publisher, January 2005.
- [b5] **G. Giustolisi, G. Palumbo**, *Introduzione ai Dispositivi Elettronici*, Franco Angeli, ottobre 2005.
- [b6] **G. Palumbo, D. Pappalardo**, "Charge Pumps for LCD Drivers" in D. Cristaldi, S. Pennisi, F. Pulvirenti, *Liquid Crystal Display Drivers (techniques and circuits)*, Springer, pp. 237-266, May 2009.
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