A 100-mW Fully Integrated DC-DC Converter with Double Galvanic Isolation

Radio Frequency Advanced Design Center

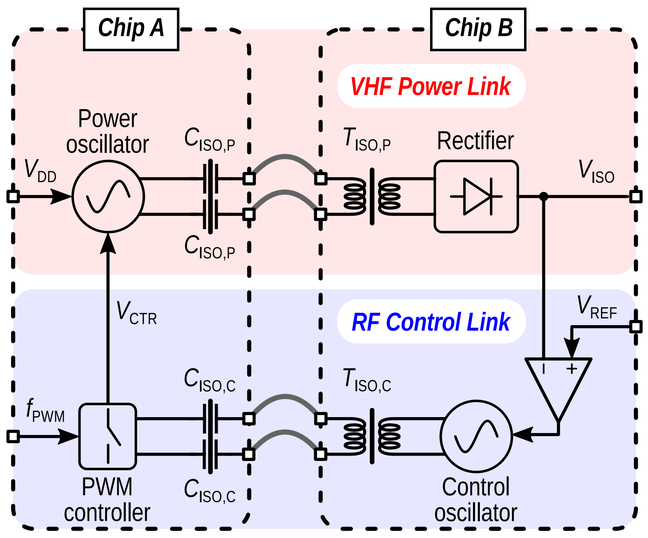
Ph.D. Student: Nunzio Greco — **Tutor: Prof. Giuseppe Palmisano**

Ph.D. Brainstorming Day - Oct. 30th 2017

I. Introduction

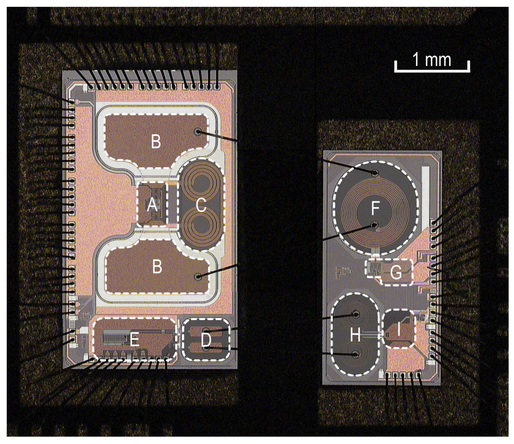
Galvanic isolators have gained a considerable interest during the last years. Isolation guarantees safety of human operators, preserves operation when a ground shift occurs, and prevents circuitry damages against hazardous voltages. Traditional isolators are going to be replaced by low cost miniaturized systems based on micro-scale isolation barriers. For such semiconductor isolators, increasing degrees of isolation were standardized. While a basic isolation guarantees protection by using only one isolation barrier, a double isolation is implemented by exploiting two isolation barriers connected in series. Double isolation provides redundancy in case one of the barriers fails, while inherently improves the overall galvanic isolation and safety level. Typically, it is the widespread approach to achieve the highest level of isolation, namely reinforced isolation. State-of-the-art integrated dc-dc converters guarantee only basic isolation. This work presents the very first 100 mW fully integrated dc-dc converter with double isolation.

II. System Description



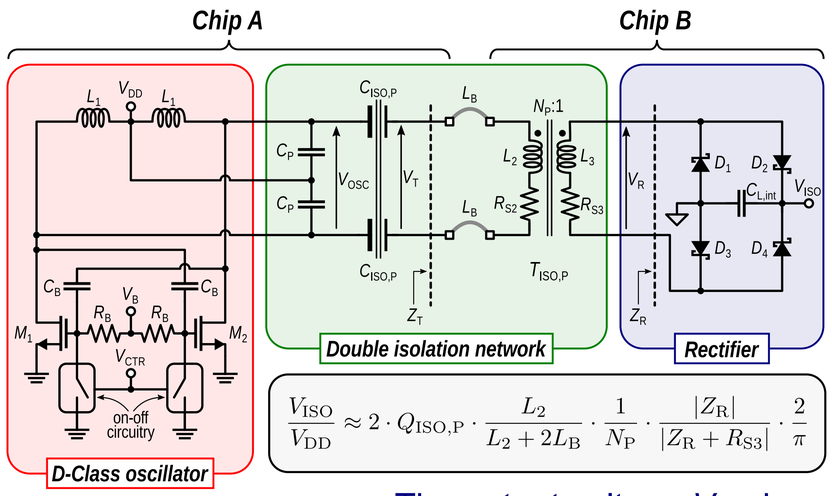
The proposed dc-dc converter consists of only two dice, both fabricated in a 0.35-μm BCD technology by STMicrolectronics. The technology features a thick-oxide back-end for 5-kV galvanic isolation.

The core of the system is the VHF power link that is made up of a power oscillator and a rectifier. A double isolation is achieved by means of an LC resonant barrier. The output voltage V_{ISO} is regulated by means of an RF feedback loop, according to a PWM control scheme, thus the duty-cycle of the control voltage V_{CTR} depends on the output error, V_{REF}-V_{ISO}. Double isolation is also guaranteed for the control feedback loop. The converter has been designed to provide 100-mW output power, P_{ISO}, with a nominal output voltage, V_{ISO}, of 3.3 V, from a 3.3-V supply voltage, V_{DD}.



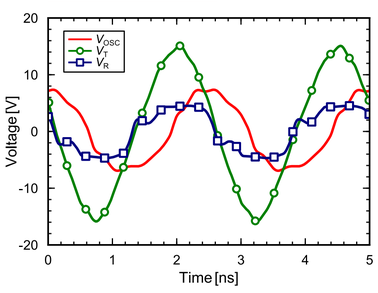
A. Power oscillator core
B. Isolation capacitors $C_{ISO,P}$ + C_P
C. Differential inductor L_1
D. Isolation capacitors $C_{ISO,C}$
E. PWM controller
F. Isolation transformer $T_{ISO,P}$
G. Rectifier
H. Isolation transformer $T_{ISO,C}$
I. Control oscillator core & Error amp.

III. Power and control links

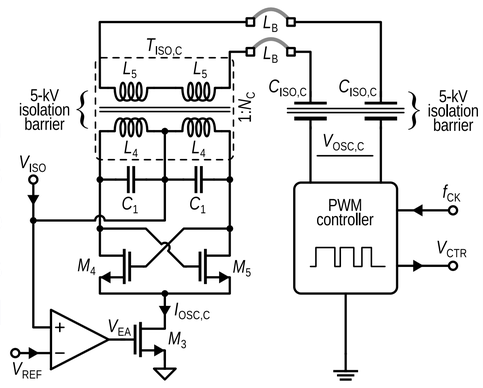


$$\frac{V_{ISO}}{V_{DD}} \approx 2 \cdot Q_{ISO,P} \cdot \frac{L_2}{L_2 + 2L_B} \cdot \frac{1}{N_P} \cdot \frac{|Z_R|}{|Z_R + R_{S3}|} \cdot \frac{2}{\pi}$$

The architecture of the power link presents several differences with respect to the ones commonly adopted for basic isolation. Double isolation is performed by means of a hybrid coupling based on the thick-oxide capacitors, $C_{ISO,P}$, and the transformer, $T_{ISO,P}$. This approach inherently enables the resonant mode operation between the oscillator and the isolation network. Unfortunately, thick-oxide capacitors exhibit heavy parasitic capacitances, C_P, that greatly limit their use in a typical power link based on a transformer-loaded oscillator. To overcome this drawback, a novel circuit architecture is proposed, which includes the parasitic capacitances into the resonant tank of an inductive-loaded oscillator, thus neutralizing the power partitioning between $C_{ISO,P}$ and C_P.

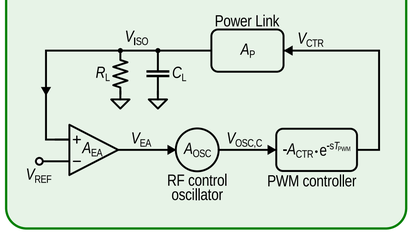


The output voltage V_{ISO} is regulated by means of an RF feedback loop. An error amplifier compares V_{ISO} with the reference voltage, V_{REF}, then its output controls the amplitude of $V_{OSC,C}$. This is converted by means of the PWM controller into a square-shaped signal V_{CTR} whose duty cycle is inversely proportional to the peak of $V_{OSC,C}$. The stability of the control loop is guaranteed by an external load capacitor, C_L, of few-microfarads.



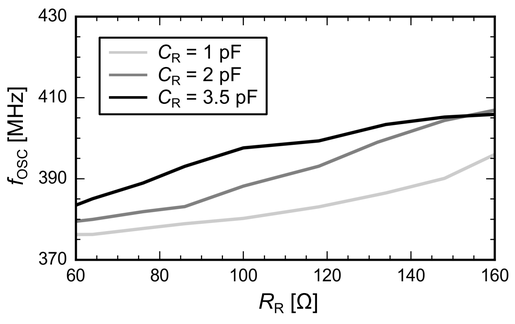
$$T_O = A_{EA} \cdot A_{OSC} \cdot A_{CTR} \cdot A_P$$

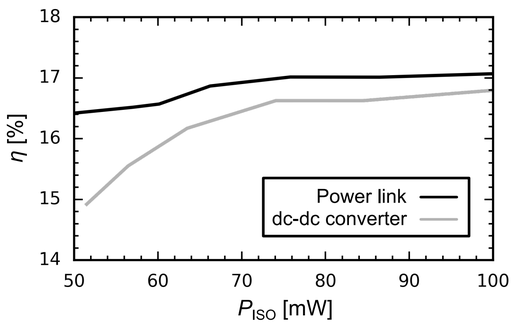
$$T(s) = T_O \cdot \frac{e^{-sT_{PWM}}}{1 + R_L C_L}$$

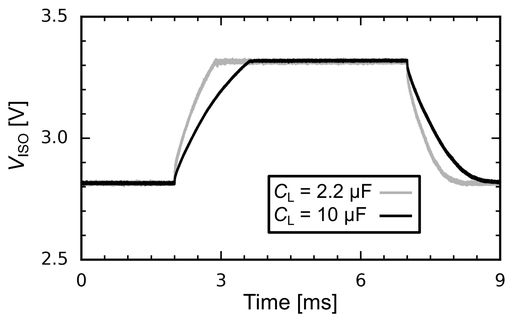


IV. Measurement

Experimental characterization was performed at room temperature and 3.3-V supply voltage, V_{DD}. Firstly, the performance of the dc–ac power conversion was evaluated measuring a variation of the oscillation frequency, $f_{OSC,P}$, less than 10% around its nominal value. The complete dc-dc converter was tested at different output power levels, while the output voltage was regulated by means of the on-chip control link. The transient response of V_{ISO} was tested with an output load of 120 Ω and a step from 2.8 V to 3.3 V of V_{REF}, which correspond to a variation of P_{ISO} from 65 mW to 90 mW. A comparison with the state of the art of fully integrated dc-dc converters with galvanic isolation was carried out. The proposed work outperform available converters in terms of isolation while achieving a remarkable efficiency and output power.







Ref.	Spina TCAS I 2015	Lombardo ISSCC 2016	Tan JSSC 2016	This work
V_{DD} [V]	5	3.3	3.3	3.3
V_{ISO} [V]	8	2	3.3	3.3
P_{ISO} [mW]	200	24	10	100
η [%]	27	10.8	24	16.8
f_{OSC} [MHz]	240	330	200	400
Control scheme/ frequency [kHz]	n.a.	n.a.	Bang-Bang/1700	PWM/100
Isolation rating	5 kV (BASIC)	5 kV (BASIC)	5 kVrms (BASIC)	2 × 5 kV (DOUBLE)
Silicon technology	0.35- m BCD, Schottky diodes	0.35- m CMOS	0.35- m DMOS, Schottky diodes	0.35- m BCD, Schottky diodes
Isolation technology	On-chip transformer	On-chip transformer	Post-processed transformer	On-chip capacitors and transformer
No. of die	2	2	3	2

N. Greco, A. Parisi, P. Lombardo, N. Spina, E. Ragonese and G. Palmisano, “A 100-mW Fully Integrated DC-DC Converter with Double Galvanic Isolation,” 43rd European Solid-State Circuits Conference (ESSCIRC), Leuven, 2017.